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An Active Inductor Based Transimpedance Amplifier with Two Local Feedbacks as a Fiber Optic Application

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ABSTRACT

An important use of active inductor feedback is reported. It was evident that a frequency dependent impedance of an active inductor is similar to that of an ordinary spiral inductor which is a key advantage in integrated circuit design given the fact that Mosfet-based active inductor circuit occupies less volume on board a chip. In this work, a 42 dBΩ transimpedance (TIA) gain at 1 GHz is obtained with 33 $pA\sqrt{Hz}$ of input referred noise with a very low power consumption of 0.605 mW. The Common-Gate Common-Source input stage with an active inductor feedback is reported in this work for the first-time long side a second stage current mirror with additional local active inductor feedback. The extremely low level of power consumption is considered to be another key advantage for that matter despite the moderate levels of TIA gain, bandwidth and input-referred noise current spectral density with 1V DC supply voltage. The LTspice software was used for simulation.

Keywords: Common-gate (CG) amplifier; Common-source (CS) amplifier; Active feedback; Current mirror.

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INTRODUCTION

For multimedia applications, high-speed, gigabit-per-second communication receivers are essential in modern communication networks. Additionally, an optical fiber communication network plays a significant role in the creation of contemporary communication systems capable of data speeds greater than Gigabits per second as an integrated low-cost system. Recent studies involved a differential low noise amplifier modified by a novel switched-gate ping-pong autozeroed architecture, an automatic phase alignment feedback, a demodulator, low-pass filter, and band-pass filter that are integrated on a CMOS chip (Lazarjan *et al.*, 2020). A capacitive feedback TIA (CF-TIA) can be used. The gain and bandwidth performance of the CF-TIA are theoretically equivalent to those of the RF-TIA (Noh, 2020).

ATIA, with a current-reuse regulated cascode (CRRGC) topology, includes an active balun and differential output drivers is reported. The TIA also includes dc current compensation, removing the requirement for bias-tees between the TIA and the photodiode (PD) (Costanzo, 2020).

This work is a continuation of previous study (Hameed, 2018) and (Al-Kawaz and Alsheikhjader, 2020) as the aim of this work is introduce an active inductor formation within two feedback loops. The active inductor is an actual replacement for an ordinary spiral inductor.

Theoretical Part

Common Gate Configuration

An amplifier stage with low input impedance is the common-gate (CG) (for field effect devices). Ignoring second-order effects in the transistors for present, the input resistance of each stage is approximately equal to $(1/g_m)$, where (g_m) represents the transconductance of the input transistor. The right choice of the bias current regarding transistor M_1 device dimensions leads to a relatively low input resistance, in which the input bandwidth can be maximized. The low-frequency circuit shown in Fig. (1) is a typical representation for (CG) input stage (Razavi, 2012).

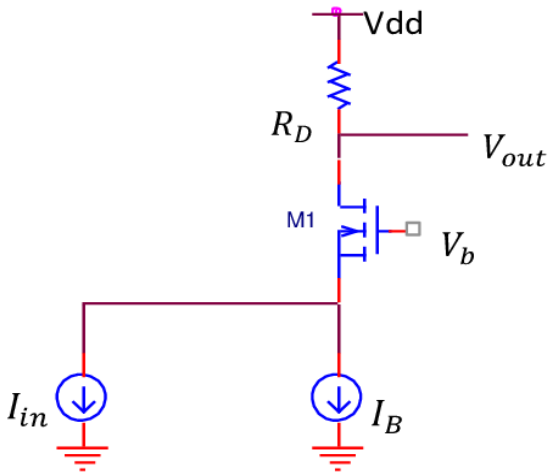

Fig. 1: Basic Common-Gate Circuit Diagram (Razavi, 2012).

Taking into account, channel-length modulation as well as body effect and assuming I_B is an ideal current source, a small-signal equivalent circuit of the (CG) stage can be assembled as in Fig. (2). The transimpedance gain is $R_T = R_D$, since all of the input current I_{in} flows through resistor R_D (Razavi, 2012).

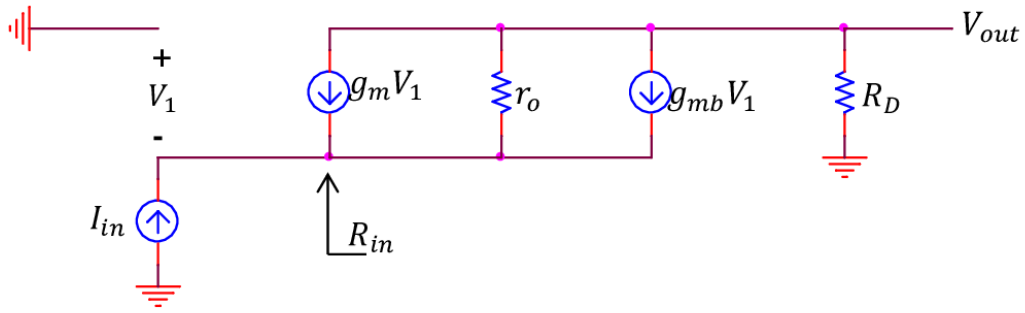

Fig. 2: Small signal model of common gate stage (Razavi, 2012).

The input resistance $-V_1/I_{in}$ is defined as the current through r_o is equal to $I_{in} + g_m V_1 + g_{mb} V_1$ it is obtained as:

$$R_{in} = \frac{r_o + R_D}{1 + (g_m + g_{mb}) r_o} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Active Inductor Configuration

It is useful to illustrate the concepts of an active inductor which will be shown in this work to have a feedback role. Consider the source follower shown in Fig. (2a), where resistor (R_S) is placed in series with the gate of (M_1). Proper choice of values can yield an inductive output impedance. Neglecting the gate-drain overlap capacitance, the source-bulk capacitance, channel-length modulation, and body effect, the small-signal equivalent circuit is depicted in Fig. (2b) (Razavi, 2012).

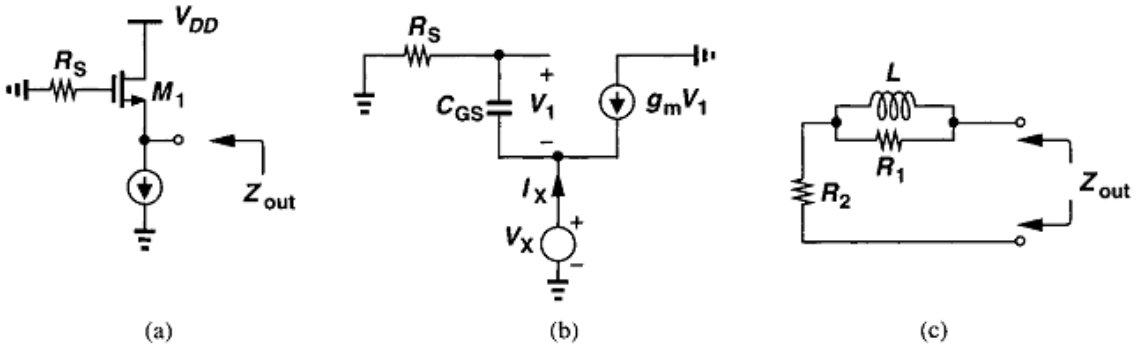

Fig. 2: (a) Source follower providing an inductive output, (b) equivalent circuit, (c) simplified network.

The output impedance general formula is (Razavi, 2012):

$$Z_{out} = \frac{R_S C_{GS} s + 1}{g_m + C_{GS} s} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Note that $|Z_{out}(s = 0)| = 1/g_m$ and $|Z_{out}(s = \infty)| = R_S$. It is therefore, if $R_S \gg 1/g_m$, then $(|Z_{out}|)$ increases with frequency, exhibiting an inductive behavior. It can be shown that under this condition the output impedance is modeled as illustrated in Fig. (2c), The transistor transconductance plays the principal role in the circuit. The output impedance frequency response depends upon the magnitude of (R_S) compared to the magnitude of $(1/g_m)$ as shown in Fig. (3) (Razavi, 2014).

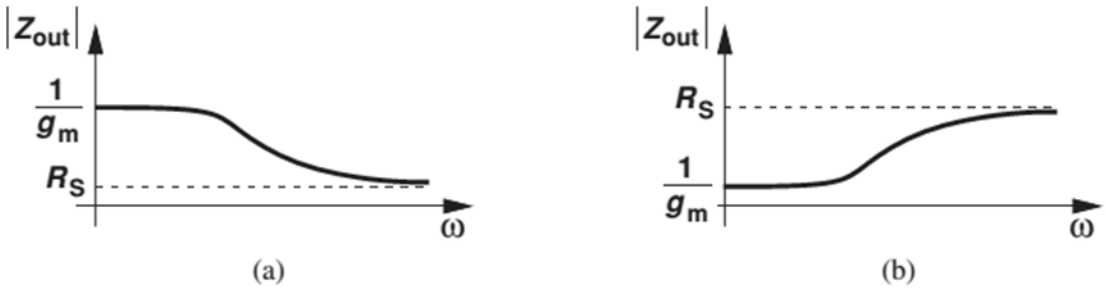

Fig. 3: Output impedance of source follower as a function of frequency for (a) small R_S and (b) large R_S.

The Design of Proposed Active Inductor Feedback Circuit

To obtain better expansion in bandwidth and achieve the objective of the research, a circuit has been proposed using transimpedance amplifier (TIA) structure with current mirror implemented in a low-voltage (1V) and (65 nm) CMOS technology as shown in Fig. (4).

The two stages proposed amplifier do have two local active inductor feedback configurations. The first stage consists of Common-Gate Common-Source (CG-CS) with two PMOS transistor based active inductor feedback represented by transistors (M_6 and M_7). This form of negative feedback involves the (CG) input stage.

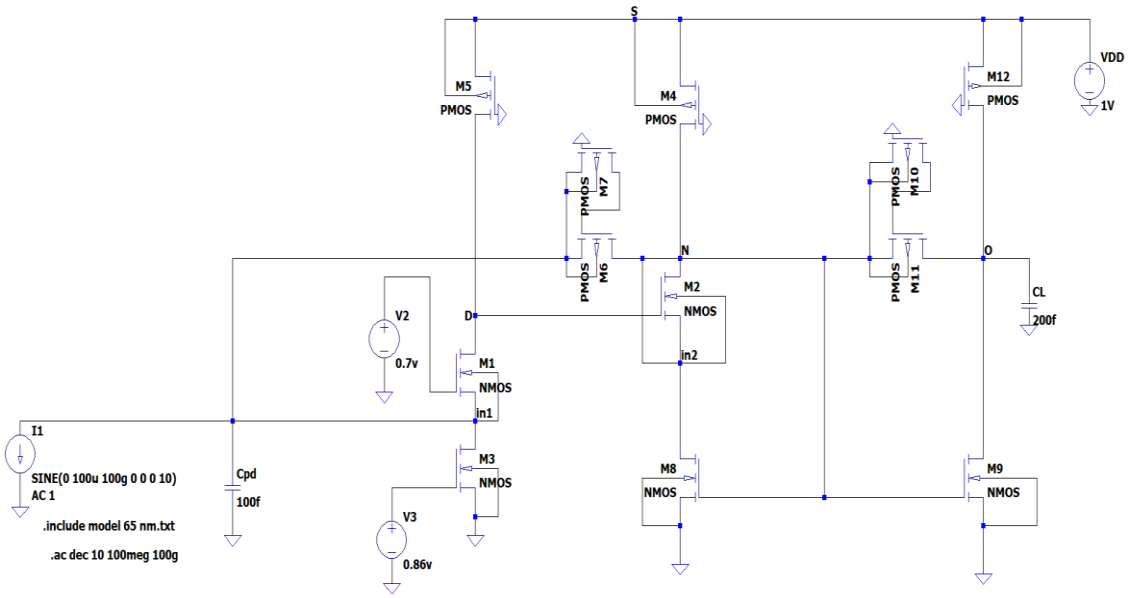

Fig. 4: Newly Proposed low-voltage TIA.

The output of the first stage is at node (N) in which it is connected to the input of the second stage. The (CG) transistor (M_2) is common between the first and second stage which is basically a current mirror one. It is interesting to point out that a second active inductor local feedback within the second stage is represented by the configuration of (PMOS) transistors (M_{11} and M_{12}).

High mobility amplifying NMOS transistors (M_1, M_2, M_8 and M_9) do have high aspect ratio (W/L) as in (Table 1), and that enables high dc drain current within a saturation configuration in which $V_{ds} \geq V_{gs} - V_{th}$. Low drain current transistors (PMOS) are being used as current sources as in the case of (M_4, M_5 and M_{12}) to provide a stable path for their drain currents and hence better dc operating point. The two active inductor local feedbacks that consist of (M_6 and M_7) and (M_{10} and M_{11}) have low aspect ratios since they are working within their triode regions.

Degeneration transistor (M_3) plays an important role in input referred noise control by varying dc biasing of its gate voltage given the fact that the drain node of transistor (M_3) is in itself the input source node of the (CG) amplifier manifested in transistor (M_1). Drain voltage of transistor M_1 provides enough voltage headroom for the common source transistor M_2 and therefore, enough drain current.

Table 1: Parameters of NMOS and PMOS transistors

n-channel	W / L (um)	p-channel	W / L (um)
M1	6.17	M4	1.3
M2	6.17	M5	1.3
M3	1.3	M6	2.6
M8	8.4	M7	2.6
M9	8.4	M10	2.6
		M11	2.6
		M12	1.3

Input Stage TIA Gain Derivation

Derivation is used and it will be followed by the simulation of the proposed circuit using LTspice Software (using pspice programming). The formulae feedback impedances represented by two local active feedback configurations are worked out in advance so that the TIA gain formula is reached. Based on the general active inductor equation (Razavi, 2014), an exclusive equation is obtained:

$$z_{f1}(s) = \frac{r_{o7} c_{gs6} s + 1}{g_{m6} + c_{gs6} s} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

The above equation is the feedback active inductor impedance of the first stage (CG-CS). It clearly involves transistors (M_6 and M_7). The output resistance of transistor M_7 including channel length modulation is given as (r_{o7}), while the main transconductance that affects this type of impedance is (g_{m6}) which is for transistor (M_6).

At low frequencies, $|z_{f1}(j\omega)|$ is equal to $(1/g_{m6})$ as this term is dominant and with no obvious role for parasitic capacitance (C_{gs6}), while its high frequencies, the time constant of ($r_{o7} C_{gs6}$) magnitude in relation to ω will determine the course of operation as to the nature of feedback impedance. Similar concept applies to the second local feedback active inductor impedance ($z_{f2}(s)$) as in eq. (4):

$$z_{f2}(s) = \frac{r_{o10} c_{gs11} s + 1}{g_{m11} + c_{gs11} s} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

The transimpedance gain of the circuit may now be calculated as shown in Fig. (4). Since the inversion amplifier's general formula is (Staric and Margan, 2006):

$$\frac{v_o}{v_i} = -A_{(s)} = -A_o \frac{S_\circ}{S - S_\circ} = -A_o \frac{\omega_\circ}{S + \omega_\circ} \qquad \ldots\ldots (5)$$

Considering (S) is the complex frequency variable., (A_o) is the amplifier open loop (DC gain). (S_o) is the amplifier (real dominant) pole, so that: $-S_o = \omega_o = 2\pi f_o$ as (f_o) is the (open loop) cutoff frequency. The sum of currents at the v_i input node is:

$$i_i = \frac{v_i}{\frac{1}{s\,c_i}} + \frac{v_i - v_o}{\frac{1}{\frac{1}{z_{f1}} + s\,c_{f1}}} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

For which $c_{f1} = c_{ds6} + c_{ds7}$, which means that active inductor feedback capacitance equals dominant capacitance of drain-to-source for (PMOS) transistors (M_6 and M_7). Assembling the TIA gain v_o/i_i , in which after simplification, the (TIA) gain for the first stage becomes as follows in which $i_i = I_{in1}$:

$$\frac{v_o}{i_i} = \frac{-A_o\,\omega_\circ \frac{(1 + s\,c_{f1}\,z_{f1})}{c_i\,c_{f6}\,r_{o6}}}{s^3 + \frac{s^2 c_i(1 + \omega_\circ\,c_{f1} z_{f1})}{c_i\,c_{f1}\,z_{f1}} + \frac{s(\omega_\circ\,c_i + z_{f1})}{c_i\,c_{f1}\,z_{f1}} + \frac{\omega_\circ z_{f1}(1 + A_o)}{c_i\,c_{f1}\,z_{f1}}} \quad \ldots\ldots (7)$$

Overall, TIA Gain Derivation

Beginning with the concept that the output current of the first stage equals the input current of the second stage, *i.e* $I_{o1} = I_{in2}$, the overall (TIA) gain formula is:

$$\frac{v_{o2}}{I_{in1}} = \frac{I_{o1}}{I_{in1}} \cdot \frac{v_{o2}}{I_{in2}} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (8)$$

Since the expression for the (TIA) gain of the first stage is:

$$\frac{v_{o1}}{I_{in1}} = \frac{Z_{o1}\,I_{o1}}{I_{in1}} \rightarrow \frac{I_{o1}}{I_{in1}} = \frac{v_{o1}}{I_{in1}} \cdot \frac{1}{Z_{o1}} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

And parallel configuration of the first stage output impedance:

$$Z_{o1} = r_{o2} // z_{f1} // r_{o4} // z_{f2}$$

The current gain of the first stage from eq. (7) becomes:

$$\frac{I_{o1}}{I_{in1}} = \frac{-A_o \omega_\circ \frac{(1 + s\,c_{f1}\,z_{f1})}{c_i\,c_{f1}\,z_{f1}}}{s^3 + s^2 A + sB + C} \cdot \left[\frac{1}{r_{02}} + \frac{1}{r_{04}} + \frac{1}{z_{f1}} + \frac{1}{z_{f2}}\right] \quad \ldots\ldots (10)$$

Note that:

$$A = \frac{c_i(1 + \omega_\circ\,c_{f1}\,z_{f1})}{c_i\,c_{f1}\,z_{f1}}\,;\, B = \frac{(\omega_\circ\,c_{i+}\,z_{f1})}{c_i\,c_{f1}\,z_{f1}}\,;\, C = \frac{\omega_\circ\,z_{f1}(1 + A_o)}{c_i\,c_{f1}\,z_{f1}}$$

In order to work out the (TIA) gain for the current mirror (second stage), a small signal model is needed according to the general formula (Phang, 2001) as follows:

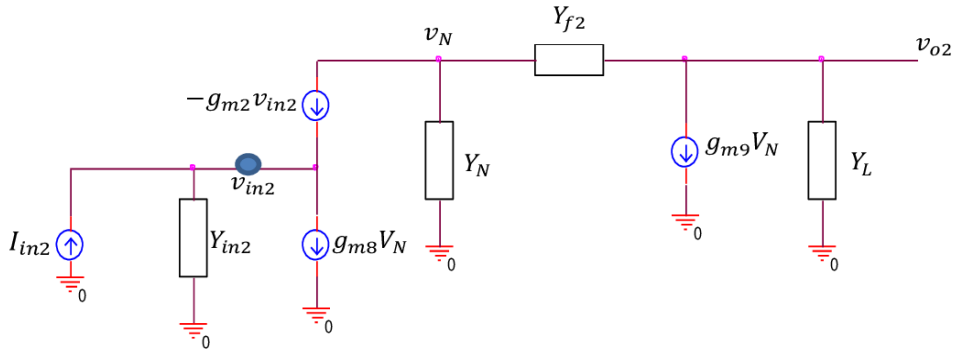

Fig. 5: A small signal model for the current mirror stage.

$$\frac{v_{o2}}{I_{in2}} = \frac{y_{f2} - g_{m9}}{\frac{y_N\, y_{in2}\, y_{f2}}{g_{m2}} + \left[\frac{y_{f2}}{g_{m2}}\, y_{in2}\,(y_N + y_L) + y_N\, y_L\right] + \left[g_{m9}\, y_{f2}\frac{y_{in}}{g_{m2}} + g_{m8}\, y_{f2} + y_{f2}(y_L + y_N)\right] + (g_{m8} + g_{m9})y_{f2}} \quad (11)$$

For which:

$$y_{in} = s(c_{PD} + c_{in}) = s\left(c_{PD} + (c_{d3} + c_{s1} + c_{s6})\right)$$

$$y_L = s(c_L + c_{out}) = s\left(c_L + (c_{d9} + c_{d12} + c_{d11})\right)$$

$$y_N = s(c_{d2} + c_{d4} + c_{d6} + c_{s11} + c_{GS8} + c_{GS9})$$

$$y_{f2} = \frac{1}{z_{f2}} + s\, c_{f2}$$

The general formula for the (TIA) gain is:

$$\frac{v_{o2}}{I_{in1}} = \frac{I_{o1}}{I_{in1}} \cdot \frac{v_{o2}}{I_{in2}}$$

Multiplying eq. (10) by eq. (11), then v_{o2}/I_{in1} which is the overall (TIA) gain formula becomes as:

$$= \frac{-A_o\omega_\circ \frac{(1 + s\, c_{f1}\, z_{f1})}{c_i\, c_{f1} z_{f1}}}{s^3 + s^2 A + sB + C} \cdot \left[\frac{1}{r_{o2}} + \frac{1}{r_{o4}} + \frac{1}{z_{f1}} + \frac{1}{z_{f2}}\right] \times \frac{y_{f2} - g_{m9}}{\frac{y_N\, y_{in}\, y_{f2}}{g_{m2}} + \left[\frac{y_{f2}}{g_{m2}} y_{in}(y_N + y_L) + y_N\, y_L\right] + \left[g_{m9}\, y_{f2}\frac{y_{in}}{g_{m2}} + g_{m8}\, y_{f2} + y_{f2}(y_L + y_N)\right] + (g_{m8} + g_{m9})y_{f2}} \quad (12)$$

TIA Bandwidth Derivation

The (CG) input stage with shunt-shunt feedback can have the formula in eq. (13) with regard to this work parameters which follow the same principles of the small signal model of Fig. (2) (Razavi, 2012). The difference in this case is that in parallel with (r_{o1}), there is an active inductor local feedback impedance (z_{f1}).

$$R_{in} = \frac{r_{o5}(r_{o1} + z_{f1}) + r_{o1}\, z_{f1}}{(g_{m1} + g_{mb1}).r_{o1}\, z_{f1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (13)$$

Total input capacitance is:

$$c_{in} = c_{pd} + c_{db3} + c_{sb1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (14)$$

The general formula for bandwidth calculation is:

$$f_{-3dB} = \frac{1}{2\,\pi\,R_{in}\,c_{in}}$$

$$f_{-3dB} = \frac{(g_{m1} + g_{mb1})\,.\,r_{o1}\,z_{f1}}{2\,\pi[r_{o5}(r_{o1}+z_{f1}) + r_{o1}\,z_{f1}].[c_{pd} + c_{db3} + c_{sb1}]} \quad \ldots\ldots\ldots (15)$$

Proposed TIA Circuit Results

The simulated proposed (TIA) circuit (using LT spice software) demonstrated the necessity of the industry's low power consumption demand for low voltage devices. The data in (Table 2) did not show that short channel effects had much of an influence. Despite the moderate TIA gain of (42 dB at 1 GHz) bandwidth, the power consumption is estimated to be extremely low at 0.605 mW as in (Table 3). The input referred noise current spectral density, on the other hand, is quite low.

We obtained excellent results in the low voltage (1V) supply (Table 2 and 3), concluding: high gain, wide bandwidth, low power consumption, and low noise at high frequencies after entering and modeling these variables for the (NMOS) and PMOS transistors**.**

Table 2: Power consumption of each transistor

Transistors	Power Consumption
M1	9.6942 uw
M2	182.73 pw
M3	64.764 uw
M4	147 uw
M5	152.48 nw
M6	91.525 uw
M7	156.4 fw
M8	79.747 uw
M9	147.01 uw
M10	6.2243 pw
M11	6.7555 uw
M12	58.676 uw
Total	0.605 mw

Table 3: Main characteristics of proposed TIA

CMOS Technology	65nm CMOS (Vth:0.7 V NMOS and -0.1 V PMOS)
Input Capacitance	100fF
Supply Voltage	1 V
Gain	42 dBΩ
Bandwidth	1 GHz
Power Consumption	0.605 mw
Input-Referred Noise	33 pA/√Hz

The (f_{-3dB}) bandwidth of (1 GHz) is validated at a gain of (42 dBΩ) in Fig. (6), which shows simulated transimpedance gain versus frequency. However, it is crucial to note that the low input capacitance of 100 fF (Femto Farad in simulation) played a significant impact in the comparatively broad bandwidth.

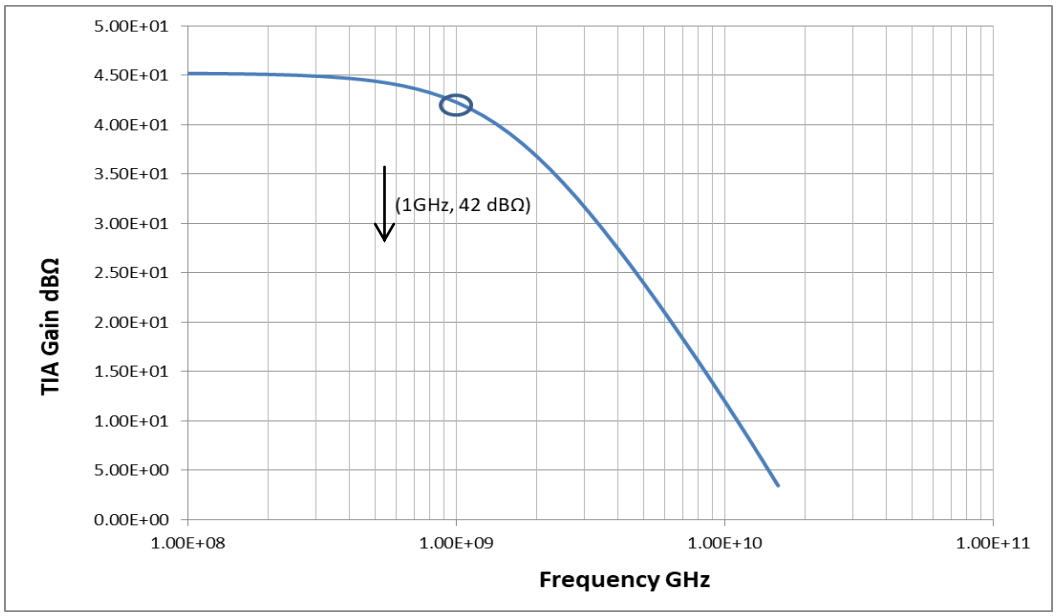

Fig. 6: Simulated TIA gain versus frequency

Fig. (7) illustrates a simulated screen shot of input impedance (left column) as function of frequency in which it reads (452 Ω at 1 GHz) point of bandwidth. This low impedance is the main characteristics of common gate key advantage that enables this wide bandwidth. The input signal faces low impedance at the source of transistor M_1 and sensed out at the drain of that particular transistor. At the right column of Fig. (7), a phase shift versus frequency that corresponds to the input impedance in which at (452 Ω) it reads approximately (145°) of phase shift with a group delay of (76.4 ps). This phase shift is due to frequency dependent parasitic capacitances associated with input capacitance (c_{in}).

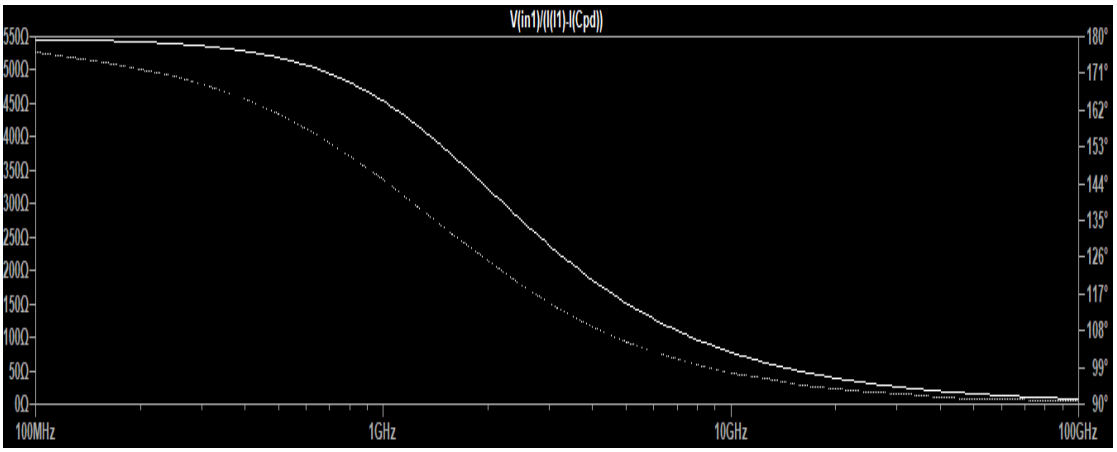

Fig. 7: Screen shot of a) LEFT: Input impedance versus frequency b) RIGHT:Input signal phase shift versus frequency

The output voltage swing range was produced by performing a (DC) sweep biasing of transistor M_1 gate from (0.7V-1V) as shown in Fig. (8). A DC biasing sweep effectively changes the overdrive voltage $(V_{GS} - V_{th})$ of transistor M_1, affecting the drain current and, as a result, the voltage gain of the common gate input stage and, as a result, the circuit's overall voltage gain. To clarify further, biasing voltage of transistor (M_1) plays a crucial role in providing enough voltage headrom $(V_{GS} - V_{th})$ and hence, establishing a clear path for drain current. Subsequently, since the Gate-to- Source voltage is affected, then, the source voltage of transistor (M_1) (drain voltage of transistor M_3) is influenced and that is clearly important in determining the input-referred noise current spectral density.

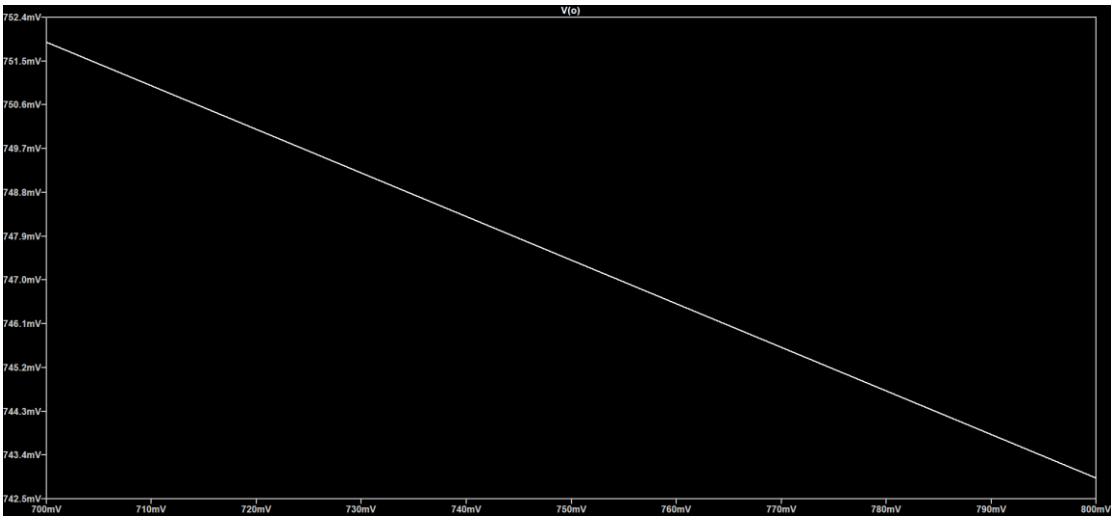

Fig. 8: DC sweep over biasing voltage of transistor M_1 from (0.7V – 1V).

In simulation, transient analysis was performed for the output voltage swing in a time domain arrangement with a maximum time period of (150 ps). The output voltage swing indicates how the transimpedance gain will change over time. As shown in Fig. (9).

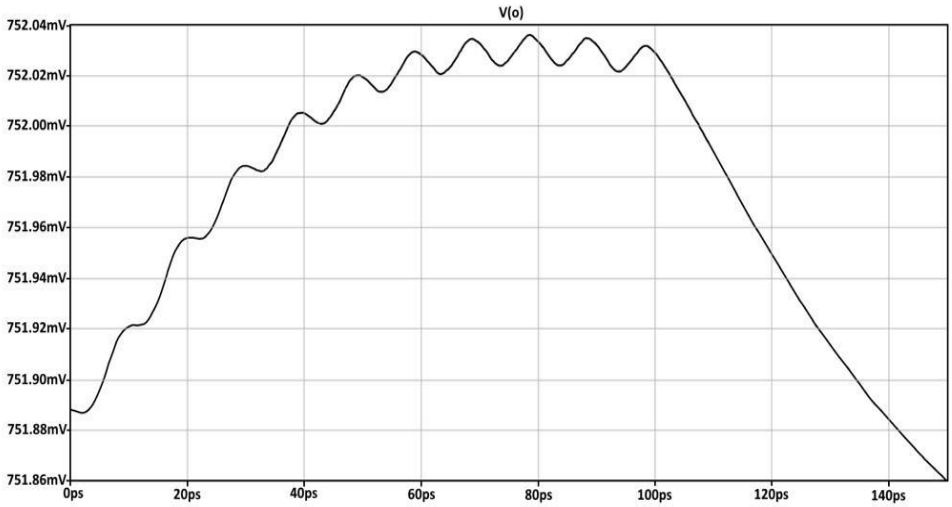

Fig. 9: Simulated time domain transient analysis of the output voltage signal. Output voltage in (mV) and time domain in (ps).

Noise Analysis and Results

For evaluating the sensitivity of the entire front-end optical receiver, the noise characteristics of the transimpedance amplifier in terms of the noise current spectral density referred to input or the matching reference noise current spectral density are critical (Sackinger, 2005). (Vanisri and Toumazou,1995). A TIA's sensitivity is also limited by its noise performance. The thermal noise is the main noise at high (TIA) bandwidth. The noise equivalent circuit model for the closed loop (TIA) topology is shown in Fig. (10). Output capacitance (c_{out}) of the (CG) input stage is manifested at the drain of transistor (M_1).

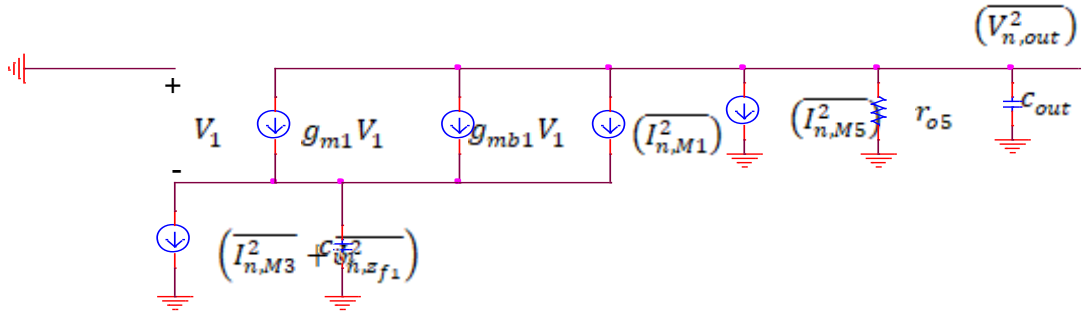

Fig. 10: Noise equivalent model of the proposed (TIA).

The Kirchhoff voltage law is applied to the noise equivalent model above according to the general formula (Razavi, 2012) to produce the total input referred noise current equation:

$$v_{n,out} = \frac{-r_{o5}\, c_{in}\, s\, I_{n,M_1}}{(c_{in}\, s + g_{mb1} + g_{m1})(r_{o5}\, c_{out}\, s + 1)} + \frac{I_{n,r_{o5}}\, r_{o5}}{r_{o5}\, c_{out}\, s + 1} \quad \ldots\ldots(16)$$

The TIA gain of the first input stage common gate general formula is (Razavi, 2012):

$$\frac{v_{out}}{I_{in}} = \frac{(g_{m1} + g_{mb1})\, r_{o5}}{(g_{m1} + g_{mb1} + c_{in}\, s)(r_{o5} c_{out}\, s + 1)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(17)$$

Dividing eq. (26) by the TIA gain given by eq. (17), it is obtained as:

$$I_{in} = \frac{-c_{in}\, s}{g_{m1} + g_{mb1}} I_{n,M_1} + \left(\frac{c_{in}\, s}{g_{m1} + g_{mb1}} + 1\right) I_{n,r_{o5}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (18)$$

From the equation above, two significant characteristics can be determined (Meyer and Blauschild, 1986). First, the noise contribution of the transistor M_1 scales linearly with input capacitance c in and input frequency. Second, because $(|c_{in}s|)$ is comparable to the amount of $(g_{m1} + g_{mb1})$, the noise delivered by (r_{o5}) to the input node does increase (Razavi, 2012). The total input referred noise current spectral density, which is calculated as a noise voltage divided by the mid band gain, can be integrated. For a frequency range of 0 to ∞, an integration of the following function is required.

$$V_{n,out}^2 = \frac{(2\,\pi\, r_{o5}\, c_{in}\, f)^2\, I_{n,M_1}^2}{[c_{in}^2(2\pi f)^2 + (g_{m1} + g_{mb1})^2][r_{o5}^2\, c_{out}(2\pi f)^2 + 1]} + \frac{r_{o5}^2\, I_{n,r_{o5}}^2}{r_{o5}^2\, c_{out}^2(2\pi f)^2 + 1}$$
$$+ \frac{(g_{m1} + g_{mb1})^2\, r_{o5}^2 \left(I_{n,M_3}^2 + I_{n,z_{f1}}^2\right)}{[c_{in}^2(2\pi f)^2 + (g_{m1} + g_{mb1})^2][r_{o5}^2\, c_{out}^2(2\pi f)^2 + 1]} \quad \ldots(19)$$

A mathematical integration of above equation and dealing with the second-order fraction of above equation as follows (Razavi, 2012):

$$\int_0^\infty \frac{4KTRdf}{(2\pi Rcf)^2 + 1} = \frac{KT}{c} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(20)$$

Then, decomposing the first and third terms of eq. (19) into partial fractions and carrying out the integration with the aid of eq. (20), and if the input pole is assumed to be dominant, *i.e.*, $c_{in}/(g_{m1} + g_{mb1}) \gg r_{o5}\, c_{out}$, then

$$V_{n,out,tot}^2 \approx \frac{KT(g_{m1}\, r_{o5}\, \gamma + 1)}{c_{out}} + \frac{2KT(g_{m1} + g_{mb1})(g_{m3} + 1/z_{f1})\, r_{o5}^2\, \gamma}{c_{in}} \quad ..(21)$$

Since for short- channel MOSFETS, $\gamma > 1$, it is reasonable to assume that $g_{m1} r_{o5} \gamma \gg 1$. Dividing both sides by (r_{o5}^2) yields the total input-referred noise current:

$$I_{n,in,tot}^2 \approx \frac{K\, T\, g_{m1}\, \gamma}{r_{o5}\, c_{out}} + \frac{2KT(g_{m1} + g_{mb1})(g_{m3} + 1/z_{f1})\, \gamma}{c_{in}} \quad \ldots\ldots\ldots\ldots\ldots\ldots (22)$$

The input referred noise current spectral density as a function of frequency is simulated in Fig. (11), with a $(33\, pA/\sqrt{H_z})$ reached at the (1 GHz) bandwidth point. This is one of the lowest values ever reported for the bandwidth in question.

The input referred noise data report is confirmed by a comparison circuit performance analysis with other research work, as shown in (Table 4). It's worth noting that the main benefit was realized, namely, a power consumption of only 0.605 mW which is amongst the lowest reported so far involving active inductor feedbacks. For determining original circuit performance data, this combination is critical.

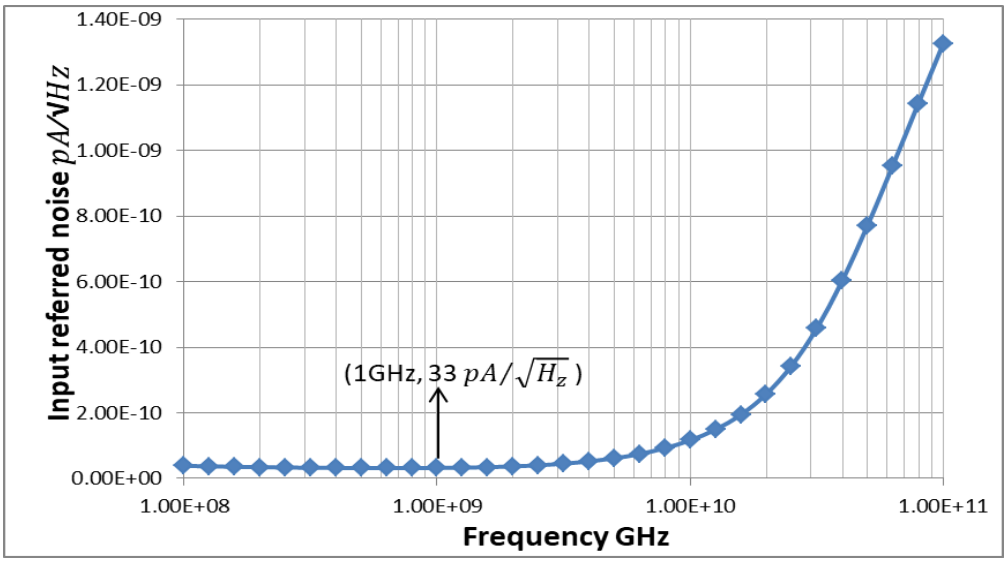

Fig. 11: Simulated input-referred noise.

Table 4: Performance comparison between the proposed (TIA) and other design works.

Researchers	Technology (CMOS)	Gain (dBΩ)	Bandwidth (GHz)	Power Consumption (W)	Input Capacitance (fF)	Supply Voltage (V)	Input Noise (pA/√Hz)
(Rakideh, *et al.*, 2016)	0.18 μm	58	8.1	34.8 m	300	1.8	15
(Chen D, *et. al.*, 2013)	0.18 μm	46	8	31.5 m	250	1.8	40
(Taghavi, *et. al.*, 2015)	0.13 μm	50.1	7	7.5 m	250	1.5	31.3
(Andre and Jacobus, 2016)	0.13 μm	54	11.5	45 m		1.5	6.8
(Honda, *et. al.*, 2016)	0.13 μm	72	38.4	261 m		3.3	14.8
(Hui, *et. al.*, 2011)	0.35 μm	54.2	2.3	58 m	500	3.3	18.8
(Seifouri, *et. al.*, 2017)	0.18 μm	59	7.9	18 m	300	1.8	23
(Chen Y, *et. al.*, 2017)	0.13 μm	83.7	32.1	150 m		3.3	
(Chen and Yang, 2016)	0.18 μm	55-69	1	6 m		1.8	9.33
This Work 2022	65 nm	42	1	0.605 m	100	1	33

DISCUSSION

At the bandwidth point, the dominant pole of this frequency response appears. The dominant pole in Fig. (6) is due to the direct effect of the input capacitance and input resistance manifested in eq. (15). The effect of pole zero may not have a direct effect on the circuit's cut off frequency. The input photodiode capacitance, which is in parallel with the input stage (i.e. the source of transistor M_1) in a common-gate design, is the most effective. The rationale for adjusting this transistor's (DC) biasing as in Fig. (8), is that transistor (M_1) source is the circuit input terminal, which determines how far the signal may be amplified initially and affects circuit bandwidth through input parasitic capacitance as shown in eq. (14). Furthermore, the source of transistor (M_1) represents the other end of the local active inductor (transistors M_6 and M_7), which has a significant impact on the negative feedback process. Needless to mention, transistor (M_7), which is the second stage's local active feedback, is also coupled to the local active inductor feedback via node (N). (transistors M_6 and M_7). With regard to transient analysis of Fig. (9), the signal from input to output is subjected to series-parallel parasitic capacitances at high frequencies, resulting in this waveform. Because these capacitances resist any rapid voltage shift across them, a (discontinuous) voltage change demands an infinite current, which is physically impossible. Furthermore, The current via these parasitic capacitances changes instantly as a result of this rapid shift in voltage. At the output node, there is an (RC) time constant that plays a role in influencing the frequency response of the (TIA) gain. Gain may fall if the (RC) time constant falls short of the predicted bandwidth.

An average low power consumption of 0.605 mW can be easily compared with other research work in (Table 4). It is considered one of the lowest reported so far, however, the use of local active feedback led to even lower power consumption. Nevertheless, the idea of applying active inductor feedback is not implemented in literature stated in (Table 4) except in this work. Despite of the fact that moderate results were obtained, low power consumption is an important step in any case. At this level of process technology (65 nm CMOS), input capacitance (c_{in}) and $(r_{o5}c_{out})$ time constant can still play an important role according to eq. (22) of the integrated input referred noise current. Active inductor feedback admittance $(1/z_{f1})$ does have an impact on the noise level involved. A $(33\,pA/\sqrt{H_z})$ is registered and that is due to the fact that (for instance), at low frequencies, $(|z_{f1}| = 1/g_{m6})$ as in eq. (3).

The moderate rise in input referred noise and power consumption (compared to a single NMOS transistor) when active inductor feedback is used is mainly because it is considered to be a feedback load on degenerated input with transistor M_3. The 1V (DC) supply voltage is consumed with a voltage drop on $(|z_{f1}| = 1/g_{m6})$ in parallel with (r_{o3}). This parallel arrangement is with the output resistance (r_{o1}) of the amplifying transistor (M_1). Active inductor feedback admittance (Y_{f2}) of Fig. (5) contributed to 0.605 mW of power consumption. Finally, these competitive results when shown in (Table 4) compared to available literature are considered to be useful to a great extent given the demand for energy efficient circuits.

CONCLUSION

It is reported that active inductor feedback is used extensively. It was clear that an active inductor's frequency-dependent impedance is comparable to that of a standard spiral inductor, which is a major benefit in integrated circuit design given that Mos-based active inductor circuit take up less space on a chip. The result is an extremely low power consumption of 0.605 mW and a (42 dB) transimpedance (TIA) gain at (1 GHz) with $(33\,pA/\sqrt{H_z})$ of input reference noise. This paper is the first to describe a Common-Gate Common-Source input stage with active inductor feedback alongside a second stage current mirror with extra local active inductor feedback.

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مكبر الممانعة البينية ذو الملف الفعال بتغذيتان استرجاع محليتان كتطبيق لليف البصري

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الملخص

في هذا العمل تم استخدام الملف الفعال في التغذية الاسترجاعية حيث كان واضحا بان سلوك ممانعة الملف الفعال المعتمدة على التردد هي مشابهة لسلوك ملف حلزوني اعتيادي وهذه الخاصية ذات فائدة كبيرة في تصميم الدوائر المتكاملة خصوصا وان الدوائر المؤسسة باستخدام ترانزستور موسفيت تحتل حجما اقل على شريحة الدائرة المتكاملة. في هذا العمل تم الحصول على ربح ممانعة بينية مقداره 41 dBΩ وعرض حزمة 1GHz وبضوضاء مرجعية الدخل مقدارها $33\ pA/\sqrt{H_z}$ وباستهلاك قدرة واطئ للغاية مقداره 0.605 mW. في هذا البحث تم تصميم مرحلة دخل بوابة مشتركة ومصدر مشترك بتغذية استرجاع محلية ذات ملف فعال ولأول مرة مع مرحلة ثانية (مرآة التيار) ذات ملف فعال بتغذية استرجاع محلية اخرى. ان المستوى الواطئ للقدرة المستهلكة يعتبر ميزة اضافية كبيرة على الرغم من المستويات المعتدلة لربح مكبر الممانعة البينية وعرض الحزمة وكذلك لتيار ضوضاء مرجع الدخل ذو الكثافة الطيفية وبمصدر 1 فولت كفولتية تغذية مستمرة. في هذا العمل تم استخدام برنامج LTspice لمحاكاة الدوائر الالكترونية.

الكلمات الدالة: مكبر البوابة المشتركة (CG)، مكبر المصدر المشترك (CS)، تغذية الاسترجاع الفعالة، مرآة التيار.