Determination Of The Memory Switching Action In CdS/SiO/CdTe Structure

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Abstract

In this paper, an experimented study is presented which determines the memory switching criterion for CdS/SiO/CdTe devices. The dc. characteristics obtained from isolated devices on various glass substrates, but having the identical CdS and CdTe semiconductors with different sandwiched SiO thicknesses reveal that the device impedance at OFF state is almost determined by the tunnel oxide thickness. But the forward and reverse threshold voltages are determined by the top contact area of the device. Physical arguments are presented which adequately explain the experimental results in this paper.

Keywords: switching, semiconductor devices and materials.

تحديد عمل المفتاحية الذاكرية في التركيبة CdS/SiO/CdTe

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الخلاصة

في هذا البحث كانت هنالك دراسة عملية لتراكيب من CdS/SiO/CdTe و التي أظهرت خواص المفتاحية الذاكرية. لقد تم الحصول على خواص مستقرة لنماذج مصنعة على قواعد زجاجية مختلفة فيها طبقات من CdS و CdTe متماثلة ولكن فيها طبقات نفقية من SiO لها أسماك مختلفة. لقد بينت الدراسة بأن الممانعة في حالة (OFF) للنبيطه تعتمد بشكل كبير على سمك الطبقة النفقية للأوكسيد, بينما مقدار فولتية العتبة الأمامية و العكسية يعتمد بشكل أساسي على مساحة طبقة التماس الفوقية. ان التغيرات الفيزيائية تبين بشكل واضح النتائج العملية في هذا البحث.

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Introduction:

Switching in amorphous devices can be divided into two clases[1]: Threshold switching devices and memory switching device, A threshold switching device is a device that exhibits threshold switching changes from its OFF state to its ON state if the applied voltage exceeds a threshold value. If the ON state then falls below a hold point (I_h, V_h) the device reverts to its OFF state. This device is non-permanent or volatile, as it always reverts to the OFF state in the absence of an applied bias.

In a device that exhibits memory switching, both the ON state and OFF state characteristics extrapolate through the I-V origin. The ON state is thus retained once the bias is removed, giving a permanent or nonvolatile, memory action, as illustrated in Fig.(1). Digital memory switching is reversible: by applying a negative bias the device can be switched from conducting ON state back to the OFF state.

The Semiconductor/Insulator/Semiconductor (SIS) has received wide attention because of its bitable latching characteristics. The SIS performs the function of an electronic memory switch in that it exhibits two stable states separated by an unstable negative resistance region. The ratio of the resistance of the two states is typically in the order of 10^4 [1]

Resistance switching behavior has been observed in amorphous silicon (a-Si) devices since the 1980[1], [2]. A typical device consists of two metal layers sandwiching an a-Si layer serving as the storage medium and results in a metal/a-Si/metal (M/a-Si/M) layered structure. As a results, few studies have been attempted on a-Si resistance switching devices as ultrahigh-density memories[2]. The integration and optimization of the glass super substrate with the CdS/CdTe semiconductor and with the contact metals is a very challenge task [3].

When the device is in the OFF state, it is characterized by a large device voltage and a low device current. In this state the semiconductor under the oxide is deep depleted since any minority charge at CdTe/SiO and SiO/CdS interfaces away by the tunnel oxide [4].

At the switching point (defined by the forward threshold voltage, V_{THF}), the device becomes unstable due to the initiation of the regenerative feedback mechanism [5], which collapses the width of the deep depletion region to its strong inversion value[6]. The device is now in the low-impedance ON state. The point at which the device switches back to OFF state is designated the reverse threshold voltage point see Fig.(1).

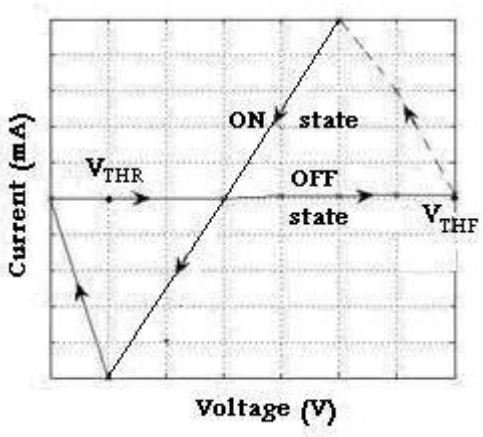

Fig.(1) I/V characteristics for SIS device, showing forward threshold voltage V_{THF} and reverse threshold voltage V_{THR} on the curve.

Device Fabrication:

Fabrication of Al, CdS, SiO, and CdTe thin films were carried out by vacuum evaporation technique using Balzers BA510 coating system.

The preparation for thin film fabrication must be done before running the system to start a certain evaporation process. Optimized fabrication parameters were determined for each type of thin film layer. Then a corresponding program was set to fabricate that layer with the required thickness.

After the preparations mentioned previously have been done, the material to be evaporated is loaded in a suitable source boat. The chamber is closed and the pumping station is switched on via the control unit. When the pressure inside the chamber reached an optimum value, early decided, the evaporation process was carried out. Using tungsten boat and Al with purity 99.99%, a thin film Al of 2000°A thickness was deposited on the micro-glass at vacuum $6*10^{-5}$ mbar for bottom contact.

Then a thin film CdTe of 5000°A thickness was deposited at vacuum of $7*10^{-5}$ mbar molybdenum boat with granules of CdTe of purity 99.99%was used for evaporation of CdTe. And the thin films of SiO(with thickness : 15°A, 20°A, and 25°A) were deposited on CdTe film at vacuum of $5*10^{-5}$. For this evaporation process molybdenum boats were used with granules of SiO of purity 99.99% as a source of evaporation.

A thin film of CdS with 5000°A thickness was deposited on SiO film at vacuum of 10^{-4} mbar. Tungsten boat with tablets of CdS of purity 99.99% were used as a source of evaporation. In the final step Aluminum top contacts with different areas of (0.03, 0.05, 0.07 and 0.09) cm2 having 2000°A thickness, were deposited.

Results and discussion:

The experimental I-V curves for each set of devices in the (OFF state) and ON state are illustrated and discussed as follows: All electrical properties reported here were characterized by current-voltage measurements. Fig.(1) shows a typical current-voltage curve, initially the device was in a very high impedance (OFF state) and it changed to a low impedance (ON state) after an initial forming process which consisted of the application of a voltage of more than V_{THF} to the top electrode. The formed device remained at (OFF state) until the application of the voltage of more than V_{THR} to the bottom electrode.

The I-V characteristics of the various devices with SiO film of 15°A thickness and with different Aluminum top contact areas are shown in Fig.(2). They reveal that as the contact area increases the switching voltage increases. This happens because for large areas the distributed voltage for each small element area will be less. Then the voltage needed for punch-through will be larger.

The sample reveals a nonvolatile memory switching device. Fig.(2) shows a typical set of static (dc) characteristics measured point by point. Immediately after forming the device is in its (ON state). The (ON state) current of 25mA or more are generally observed. On increasing the reverse potential (i.e. a voltage applied to the bottom contact with respect to top contact) a revere threshold voltage V_{THR} is reached beyond which the device switches to an (OFF state) with resistance of the order 1MΩ

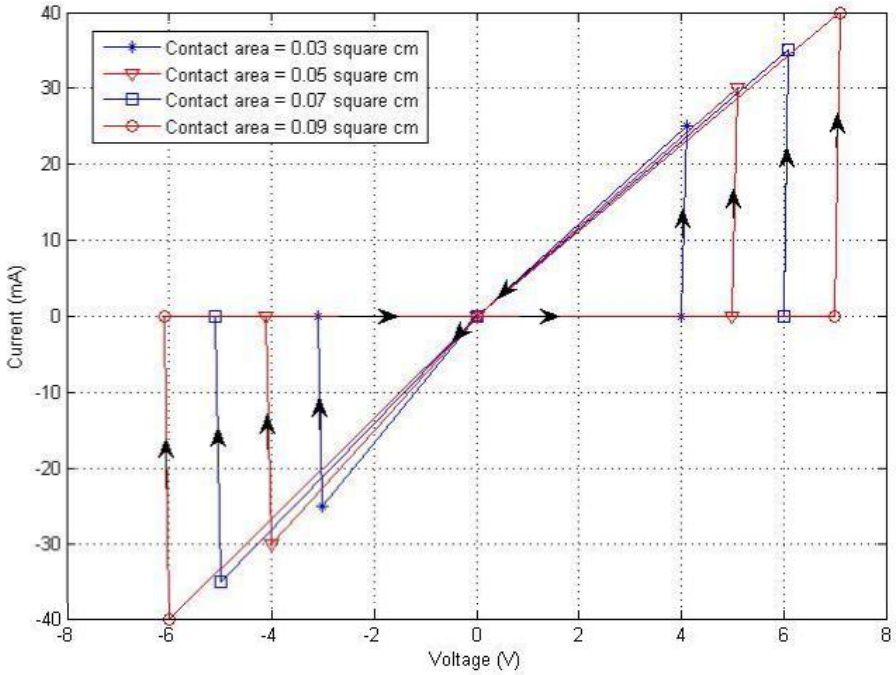

Fig.(2) I/V characteristics of CdS/SiO/CdTe structure with SiO thickness of 15 ^{O}A

The reverse threshold voltages are V_{THR} = -3, -4, -5, and -6v for the particular batch of specimens with top contact areas of 0.03, 0.05, 0.07, and 0.09cm^2 respectively. The OFF state is stable for voltage range of V_{THR} to V_{THF}. If now the forward potential is increased beyond a value of V_{THF}, the forward threshold voltage (V_{THF}), the device switches back into its high conductivity (ON state), The forward threshold voltages are V_{THF} = 4, 5, 6, and 7v for the specimens with top contact areas of 0.03, 0.05, 0.07, and 0.09 cm^2 respectively.
As noted above, the OFF state impedance is of order 1MΩ for specimen with SiO thick of 15^{o}A having different top contact areas.

The experimented I-V curves for the set of devices shown in Fig.(3) illustrate the memory switching action for the specimen with SiO of 20°A thickness. The forward threshold voltages V_{THF} = 4.5, 5.5, 6.5, and 7.5v for the specimens having top contact areas of 0.03, 0.05, 0.07 and 0.09 cm^2 respectively. While the reverse threshold voltages are V_{THR} = -3.5, -4.5, -5.5, and -6.5 for the top contact areas of 0.03, 0.05, 0.07 and 0.09 cm^2 respectively. The OFF state impedance in these specimens is in order of 2MΩ.

Fig.(4) shows the experimental I-V curves for the devices with SiO thickness equal to 25^{o}A. It seems that the forward threshold voltages are V_{THF} = 5, 6, 7, and 8v for the samples having top contact areas of 0.03, 0.05, 0.07, and 0.09 cm^2 respectively. While the reverse threshold voltages are V_{THR} = -4, -5, -6, and -7v with the same respect of top contact areas above. The OFF state impedance in these samples is about 3MΩ.

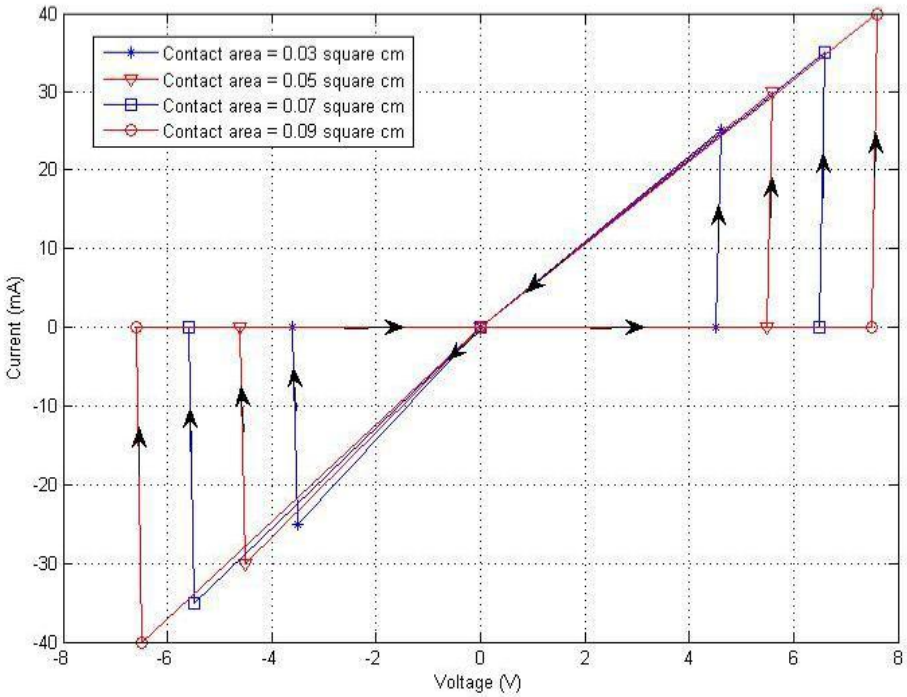

Fig.(3) I/V characteristics of CdS/SiO/CdTe structure with SiO thickness of 20 ^{O}A

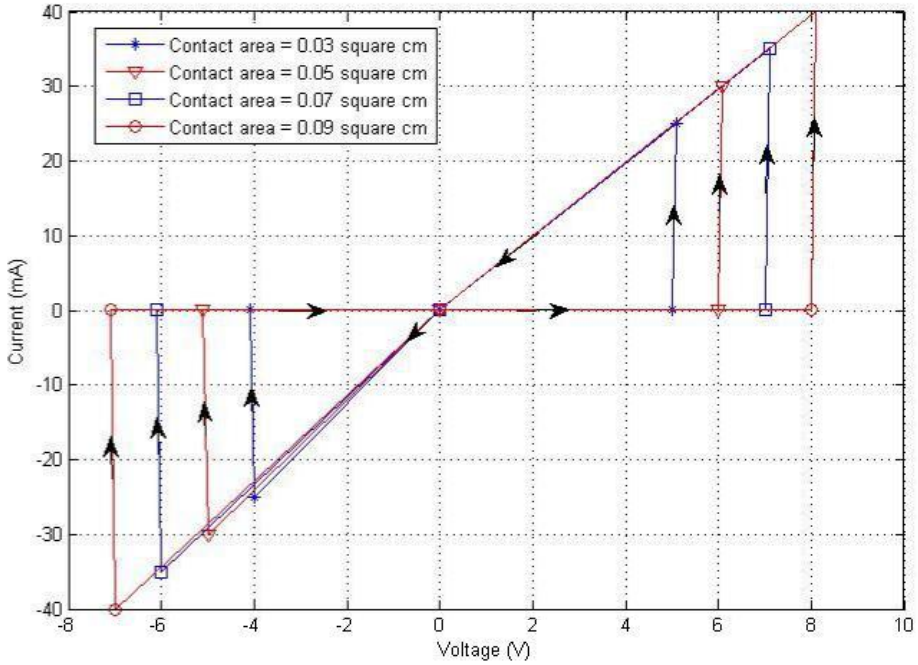

Fig.(4) I/V characteristics of CdS/SiO/CdTe structure with SiO thickness of 25 ^{O}A

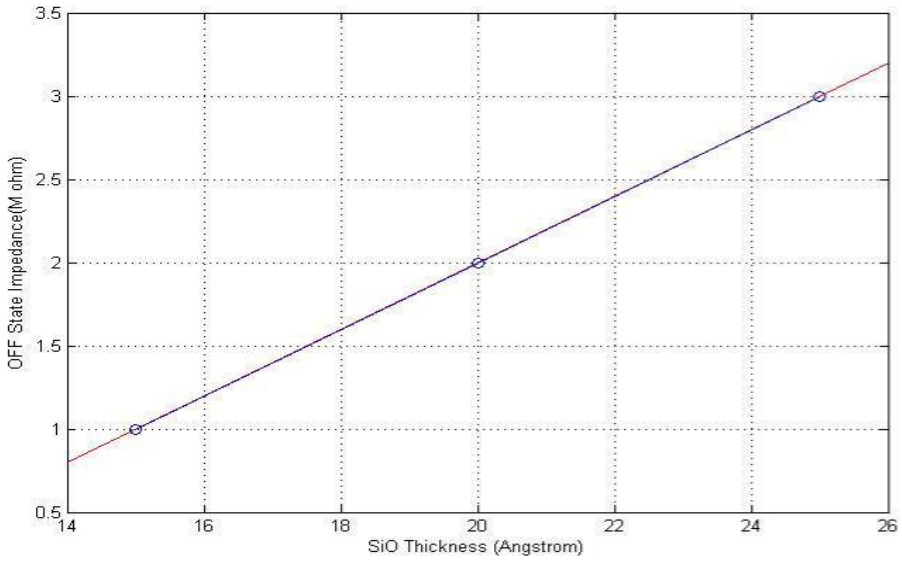

Fig.(5) SiO thickness versus the OFF state impedance of CdS/SiO/CdTe structure

Fig.(5) reveals the direct proportionality between SiO thickness and the OFF state impedance. It is seen that the switching current becomes less for thicker tunnel oxides as would be expected [1].

Fig.(6) points out that the forward and reverse threshold voltages are proportional directly with the top contact areas. It is experimentally shown that a reduction in isolated junction area results in a lower magnitude of switching threshold voltage. This is due to improved injection efficiency at the various layers interfaces [7].

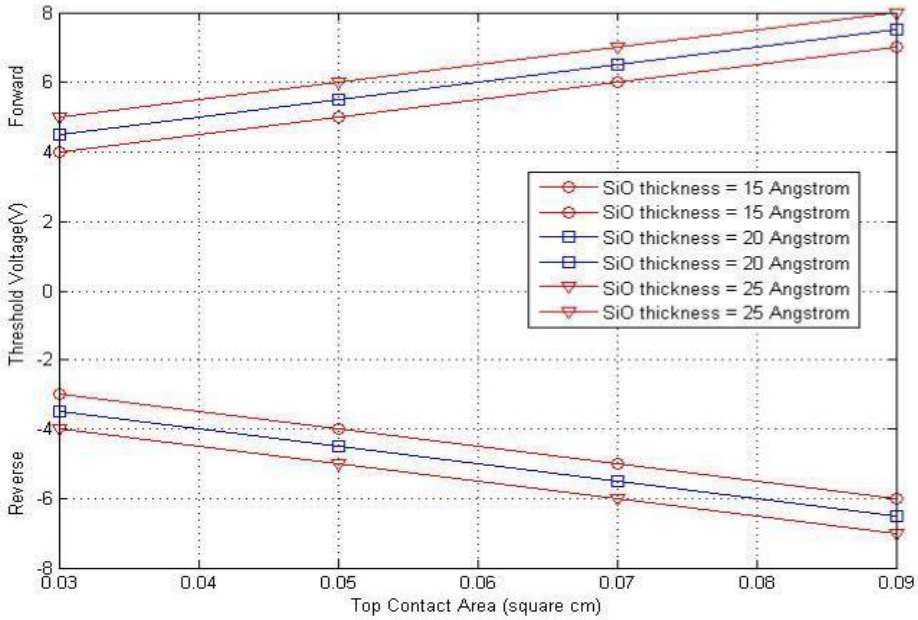

Fig.(6) threshold voltages versus top contact area of CdS/SiO/CdTe structure

Conclusion:

In this paper we present experimental results which strongly suggest that the device impedance is primarily oxide controlled. In particular for a given tunnel oxide thickness, the forward threshold voltage point is characterized by an essentially constant value of minority carrier current density reaching SiO/CdTe interface. While the reverse threshold voltage point is determined by the minority current density at SiO/CdS interface [8],[9]. Furthermore, It is experimentally shown that a reduction in isolator junction area results in a lower magnitude of threshold voltages. This is due to the improved injection efficiency of the CdS/SiO/CdTe junction which consequently initiates the regenerating feedback mechanism [5], [8], well before punch-through is reached [7].

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