Neural Network Based Pipelined-Parallel Generation of PWM Signals Suitable to Drive Three Single Phase UPS

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Abstract

A reliable technique has been proposed to generate a real time pulse width modulation (PWM) signals in order to drive three – single phase uninterruptible power supply (UPS). The PWM patterns have been generated using field programmable gate array (FPGA) and based on selective harmonic elimination method. These patterns are used to drive the six of switching power transistors of the voltage source inverter to produce three – single phase UPS. In order to solve the problem of the complexity of the nonlinear transcendental equations, an intermediate steps have been taken, using artificial neural network (ANN). This will overcome the problem of the off line solution and therefore obtaining the required data to solve the obstacle solution from off line to on line. Therefore, the trained ANN is implemented in a parallel hardware by using FPGA. The benefits of using FPGA to perform ANN are promising and the technique becomes very attractive. It allows a real time, simple, fast, reliable and efficient design with low hardware costs. Finally generating selective harmonic elimination pulse width modulation (SHEPWM) patterns as a real time signals are become visible.

Keywords: Field programmable gate array, Selective harmonic elimination pulse wave modulation, Neural networks

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توليد إشارات تضمين عرض النبضة بأسلوب خط أنابيب-توازي مبني على الشبكات العصبية مناسب لسوق مصدر قدرة غير منقطع ثلاثي الأطوار

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الخلاصة

تم في هذا البحث اقتراح تقنية موثوقة لتوليد تضمين عرض النبضة (PWM) في الزمن الحقيقي لسوق مصدر قدرة غير منقطع ثلاثي الاطوار المنفردة. تُولد انماط PWM بواسطة مصفوفة البوابات المبرمجة حقليا FPGA المبنية بطريقة ازالة التوافقيات المنتقاة. تُستخدم هذه الانماط لسوق ترانزيستورات القدرة لعاكس مصدر الفولتية لانتاج UPS ثلاثي الأطوار المنفردة وتم استخدام الشبكات العصبية الاصطناعية ANN لحل مشكلة تعقيد المعادلات غير الخطية. تم تنفيذ المنظومة باستخدام التنفيذ المادي المتوازي للتغلب على عائق الزمن المستغرق عند تنفيذ المنظومة برمجياً. أصبح استخدام FPGA لتنفيذ ANN من التقنيات المرغوبة وذلك لامكانية تنفيذ المنظومة في الزمن الحقيقي فضلا عن سهولة وسرعة ووثوقية ورخص تنفيذ التصميم. وبالتالي يمكن توليد إشارات تضمين عرض النبضة بطريقة إزالة التوافقيات المنتقاة في الزمن الحقيقي.

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1. Introduction

The main element of the voltage source inverter (VSI) is the power switching devices such as IGBT, Bipolar Power transistor, Power MOSFET, GTO, etc.. The VSI is the core of various power electronic applications. Such applications are UPS, STATCOM, Active Filter, AC Drives, Arc Furnace, SMPS, LHVDC etc.. Driving these devices need certain strategy that fulfill the application. However, irrespective of the application type and the level of sophistication, the PWM inverter circuit is achieved electronically. This is performed using suitable and efficient PWM switching strategy. The PWM is a pattern signal, which can be programmed, according to certain strategy, and depending on type of the application. Therefore, PWM strategies have been developed in various approaches relating to the historical technology progress and the types of applications. Different circuits were used to generate PWM signal, which have been improved rapidly [1-5]. Different techniques may be used to obtain PWM periodic signals. Such techniques are chosen to suit the application. The main problem is to produce PWM signals to drive the UPS on line, and to generate stabilized voltage and frequency magnitudes with minimum total harmonic distortion [2]. One of the interesting PWM methods is the Selective Harmonic Elimination Pulse Width Modulation (SHEPWM), which has been used to drive different types of voltage source inverter which is the main unit for wide range of power electronic applications. This is due to its ability to eliminate wide band of specified harmonic frequency components at relatively low switching frequencies [6]. In order to fulfill the above requirements, a PWM pattern has been generated which is based on SHEPWM method. Recently this method became one of the main strategies which have been used widely [7]. The SHEPWM method was used as off line and the pattern is to be presented as a look up table. This is due to time consuming needed to solve the complexity of the set of nonlinear transcendental equations. The aim of this paper is trying to use SHEPWM as an on line method. Therefore, these equations have been solved for wide range of variation parameters [8]. The obtained results, considered as intermediate results, are trained using ANN. Then the ANN is implemented in hardware by using an FPGA and therefore on line system is accomplished. Due to the nature and layout of VSI circuit, a precaution is needed to avoid extreme dead short circuit. Therefore a modification is performed by introducing dead time, which is required to prevent the two power switching devices on each of the three legs of VSI circuit, to be conducted simultaneously. This dead time has been considered for all SHEPWM signals, to drive the six power switching devices, which have been generated by FPGA. The six generated signals drive the UPS to obtain a high quality of three-single phase stabilized power supply. The proposed system is illustrated in Fig.1.
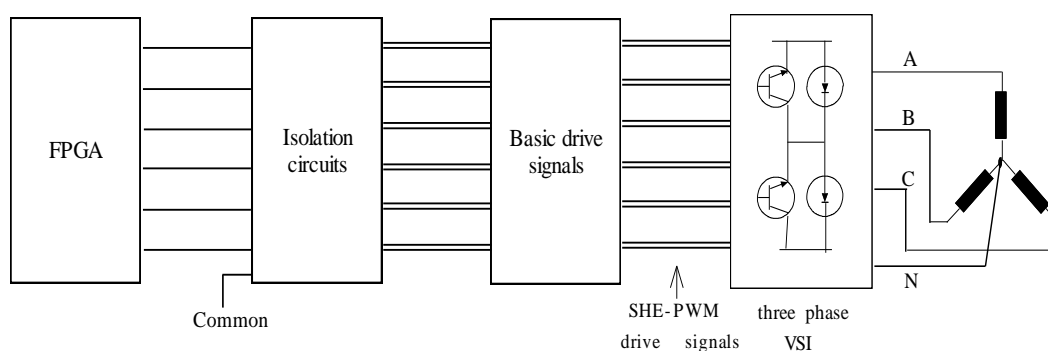

Figure (1) Three single phase load with its drive system

The above technique can be applied to supply three-phase delta or three wire star connected load.

2. Principle of Selective Harmonic Elimination PWM (SHEPWM)

In order to obtain an effective sinusoidal phase inverter voltage, a periodic pulse width modulation waveform is needed. This waveform has quarter and half switching angles symmetry. The fundamental phase inverter voltage can be adjusted with mitigation or elimination [3,4,8] of low order harmonic components by applying Fourier series. The following Fourier series represent the output phase inverter voltage, illustrated in Fig. 2.

$$\hat{V}_n = \frac{4E}{n\pi}\left[(-1)^N\left(1+2\sum_{k=1}^{N}(-1)^K\cos(n\alpha_k)\right)\right] \tag{1}$$

Where:
E is the half value of DC link voltage of VSI,
$\hat{V}_n$ is the amplitude output phase voltage of nth harmonic
order, including fundamental (n=1).
N is the number of switching angles α_k per quarter cycle.

The fundamental amplitude phase voltage $\left(\hat{V}_1\right)$ is set to rated value, while the low order harmonic components are setting to zero. Each set of nonlinear equations are needed to be solved for corresponding value of $\hat{V}_1$, as given below:

$$\left\{\begin{array}{l}\hat{V}_1 = \frac{4E}{n\pi}\left[(-1)^N\left(1+2\sum_{k=1}^{N}(-1)^K\cos(\alpha_k)\right)\right] \\ 0 = \frac{4E}{3\pi}\left[(-1)^N\left(1+2\sum_{k=1}^{N}(-1)^K\cos(3\alpha_k)\right)\right] \\ 0 = \frac{4E}{5\pi}\left[(-1)^N\left(1+2\sum_{k=1}^{N}(-1)^K\cos(5\alpha_k)\right)\right] \\ \vdots \quad \vdots \qquad\qquad \vdots \qquad\quad \vdots \\ 0 = \frac{4E}{n\pi}\left[(-1)^N\left(1+2\sum_{k=1}^{N}(-1)^K\cos(n\alpha_k)\right)\right]\end{array}\right\} \tag{2}$$

Also the following constraint transactions for the switching angles must be accomplish:(0<α₁, α₁,………,α₁<π/2).

The number of equations needed to be solved, for each selected value of fundamental voltage, is equal to number of harmonic components selected to be eliminated plus one. Different methods may be used to solve each set of nonlinear equations using numerical methods, or using recent approach was proposed by refrence[9], which based on Genetic Algorithm to obtain optimum solution. Also a suggested method is based on half wave symmetry SHEPWM which is suitable for multilevel VSI [10]. For a typical example, in order to set the fundamental voltage at certain value and eliminate the most significant harmonic orders, which are the 3rd, 5th, 7th, 9th and 11th, therefore six transcendental nonlinear equations have been solved, based on Newton Rapson approach, to determine the

switching angles for quarter cycle. Therefore for varying the fundamental voltage in step, say 0.5%, it is required to repeat solving the six of nonlinear equations two hundred times. Then two hundred sets of switching angles are obtained using numerical approach. Each set has six switching α_1, α_2,...., α_6 which represent quarter wave symmetry. Then PWM pattern for complete cycle can be deduced from symmetry for each value of fundamental phase voltage as shown in Fig.2.
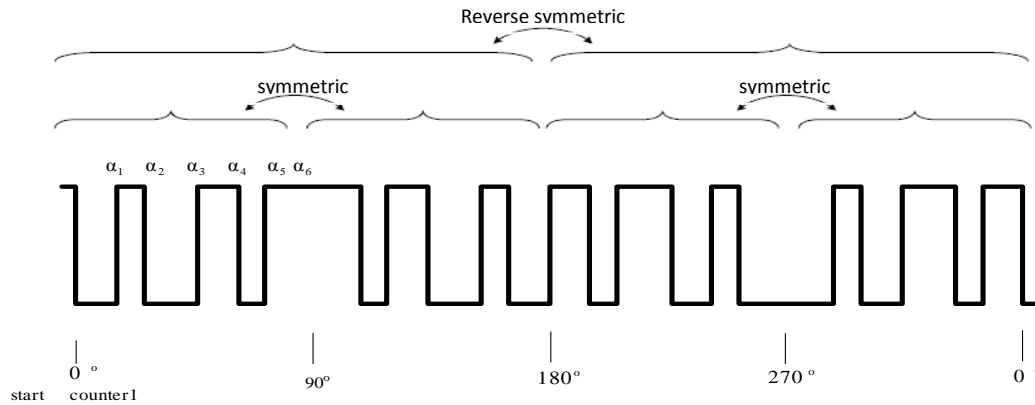
Figure(2) Symmetric property of the PWM signal

3. PWM PATTERN GENERATION BASED ON NEURAL NETWORK

SHEPWM has significant features, but the complicity of this method is to generate the PWM pattern in real time as on line according to instant variation of modulation index. Therefore it is suggested [4] to obtain all the SHEPWM patterns in off line and then using a feed forward neural network which accepts modulation index as input, M, and the output is the switching angles. The neural network has one input neuron and n output neurons (to produce n switching angles). For a typical example, six switching angles for quarter cycle is chosen, n=6, in order to eliminate five selected harmonic orders. These orders are; 3rd , 5th , 7th , 9th , and 11th . The hidden layer has number of neurons, which depend on the complex of the application and the speed of the process to reach a minimum MSE (mean square error) between the output and the desired value; the neurons have sigmoid characteristics and bias, as given. The training set for the network was produced off-line solving of equations for two hundred values of M, modulation index range between (1% to 100%). The learning and training algorithm adjust the weights and biases for ANN in order to perform the desired task. The training result to perform minimum MSE has one, ten and six neurons for input, hidden and output layers respectively (see Fig.3). The neuron functions for hidden layer are Tansig while the type functions for output neurons are linear.
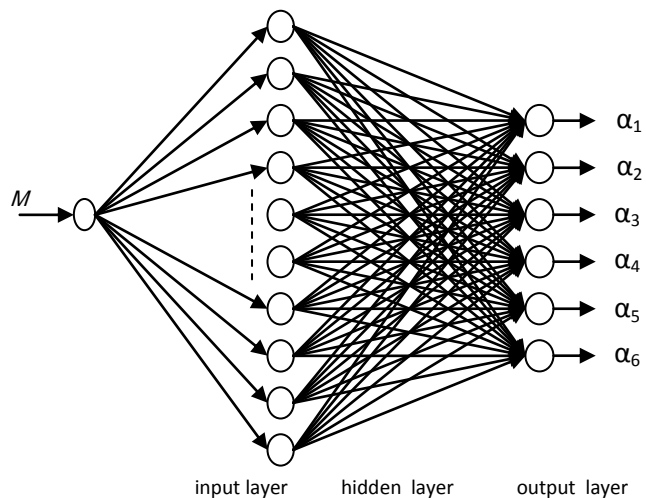
Figure(3) The layout of neural network for SHEPWM

4. Real Time Generation of PWM Signal

To generate the SHEPWM drive signals in real time, a simple, fast, reliable and efficient low costs of hardware is used. The whole system is implemented using FPGA. The design strategy is summarized as follows:

Software steps:
1. *Training the neural network by using software model on general purpose processor.*
2. *Download weights to be used in hardware model.*
Hardware steps:
3. *Implementation of the neural network by using FPGA based hardware model. Afterward, the first six switching angles are produced.*
4. *According to the quarter symmetry, the next six switching angles are produced.*
5. *According to the reverse symmetry, the last twelve's angles are produced.*
6. *Based on the steps 3,4 and 5 above, switching angles for the second and third phases are produced.*
7. *Three single phase PWM signals are generated.*
8. *Rising edge processing of the PWM signals is performed.*

The real time (hardware) part of the proposed system is explained clearly in the following sections.

5. ANN Implementation Platforms

Artificial neural network in most cases is implemented in software. The benefit is that the designer does not need to know the mathematical works of the processing elements and then concentrate on the application of the neural network. However, the disadvantage is in the low speed. The software implementation is not suitable in real time applications.

The hardware implementation of ANN has been achieved in analogue and digital techniques. Analogue implementation suffers from inexact computation results and from the lack of the reprogramability.

Application Specific Integrated Circuit (ASIC) is used in digital hardware as a solution. Both approaches (analog and digital-ASIC) have fixed topology, resulting in a design suited only for one type of target application. Digital implementation, using FPGAs, allows the redefinition of the topology using the same hardware. Hardware engineers using a Hardware Description Languages (HDL) have traditionally configured fPGAs. Very High Speed Description Language (VHDL) is one of the most efficient description languages used. The disadvantage of an implementation using FPGA over ASIC is the performance. FPGA normally run slower than ASICs.

In this paper, the neural network shown in Fig. 3 is implemented in hardware using FPGA. In this implementation, the neural network is trained *off-chip* and the convergent parameters then fed to the hardware for test and synthesis.

Fixed-point numerical representation is used in calculations. Fixed-point implementations are less complex and less area consuming than floating-point arithmetic and therefore their use helps to reduce system cost [11].

Direct implementation for non-linear Tan-sigmoid activation functions is very expensive. There are two practical approaches to approximate non-linear functions with simple FPGA designs. **Piece-wise linear approximation** describes a combination of lines in the form of $y=ax + b$ which is used to approximate the non-linear function. Note that if the coefficients for the lines are chosen to be powers of two, the non-linear functions can be realized by a series of shift and add operations. Many implementations of neuron activation functions use such piece-wise linear approximations. The second method is **lookup tables**, in which uniform samples taken from the center of non-linear function can be stored in a table for look up. The regions outside the centre of the non-linear function are still approximated in a piece-wise linear fashion.

The neural network used in this paper consists of two types of activation functions classified as linear and non-linear. Hidden layer neurons have non-linear activation functions, while the output layer activation function is linear (pureline function). Piece-wise linear implementation is used to realize the non-linear activation function as mentioned above. The pureline linear activation function is $y=ax$ and $a=1$ as shown in Fig.4, therefore the function weighted sum input will be the activation function output.
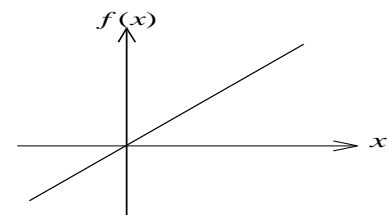

Figure (4): Pureline linear activation function

6. The Architecture of the PWM Network

The design and all of the work are geared towards the implementation of the PWM network in a modular fashion. The modular design means that the network can become as large as practically possible thus providing a structure for more complex application. The processing elements and the complete architecture of the neural network is shown in Fig. 5. The neural network has single input which represented by the modulation index (M in Fig. 3). The pipelining parallel processing technique is efficiently considered during the design session of the neural network architecture. Most multilayer neural networks require that, in order the current layer's calculations begin, the neuron's output of the preceding layer should be completed. In our work, a new technique is presented: the calculations for both layers(the hidden and output layer) are achieved concurrently as depicted in the following paragraphs.

In the first hidden layer, to reduce the hardware complexity, one multiplier is used in a pipelined fashion. Therefore, one processing element is considered. This processing element is used for all twelve neurons in a pipelined fashion. Each neuron requires one location to store its weight value and another location to store the bias value. As soon as the first value (X) is output from the saturated activation function, it is used to begin calculation in the next layer of this network.

In the other hand, each neuron in the output layer requires its own processing element. That is because each neuron in this layer is fully connected to the neurons in the preceding layer. Each neuron has twelve weights and one bias, thus, thirteen memory locations should be available for each processing element(PE) in this layer. The PE components are connected across registers, therefore they operate in pipelined fashion. The pureline activation function of the output layer is simply achieved by accumulating the neuron inputs. All neurons in the output layer are operated in parallel (Fig. 5).
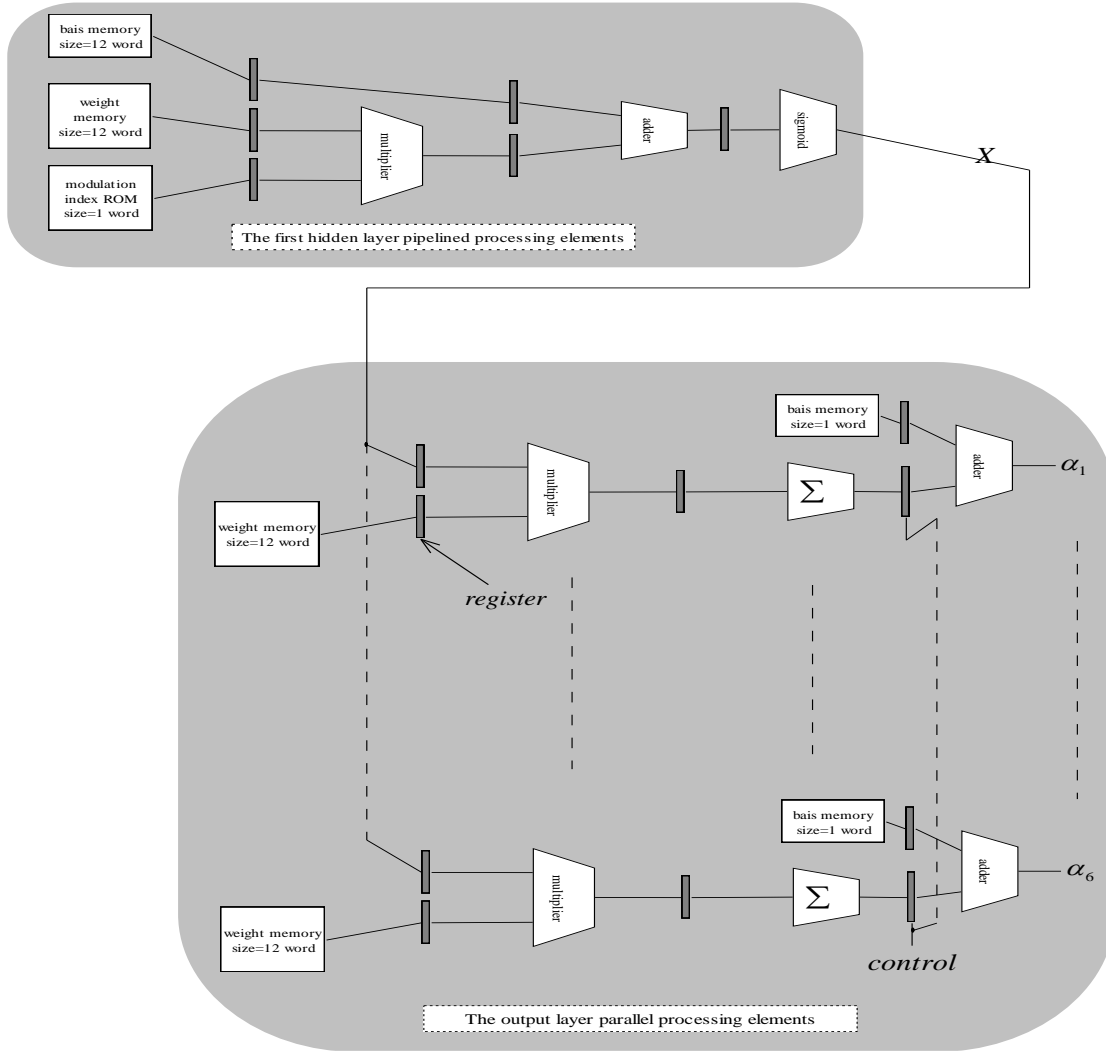
Figure (5) The complete neural network structure

As soon as the output layer calculations are completed and fundamental switching angles (α_i: i=1 to 6) values are being available, and according to the quarter-wave symmetry, the six other switching angles (α_i: i=7 to 12) is simply concluded.

Furthermore, for three phase requirements, all switching angles required for each phase can also be concluded from the six angles above. There is no need to produce six switching angles for each phase. Thus, only single neural network hardware, which is used for single phase, is also used for the two other phases. This technique depends on adding a fixed value (phase shift) for all the six switching angles to produce new six switching angles for each phase, as follows:

$$\beta_i = \{\alpha_i + \frac{2\pi}{3}\}, i = 1,.....6$$

$$\theta_i = \{\alpha_i + \frac{4\pi}{3}\}, i = 1,.....6 \tag{3}$$

Where β and θ are fundamental switching angles for the 2nd and 3rd phases respectively. Now, the same approaches (quarter-wave symmetry) are used to produce all switching angles for each phase. Finally, the last part of the designed system (the signal generator Fig(6) begins. The signal generator consists of three identical parts in addition to a global counter. Each one generates a single phase signal based on the calculation produced from eq.(3). Each part consists of two main components: counter and decoding function generator.

For each part, counter starts and end its operation according to the required function of the output signal. Each counter starts counting when a start pulse is received from the global counter as shown in Fig.6. For example, for the global counter starts function, the first phase (Φ1) counter starts operating with a zero minimum value and a maximum value equivalent to 2π. After reaching the maximum value, it starts its function again. The decoding function generator has two main components: comparator and decoder (Fig. 7). The counter starts counting until reaches the first value of the switching angel (α_1), the output signal becomes equal to p_0 as shown in Fig. 7b as soon as the first comparator fires.
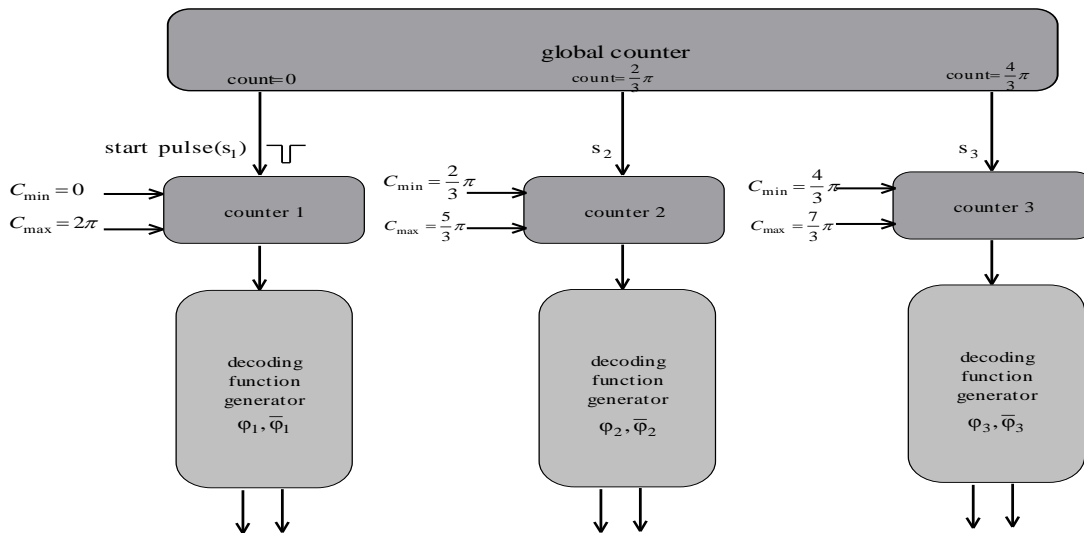

Figure(6) Three Phase signal generator


(a)

(b)
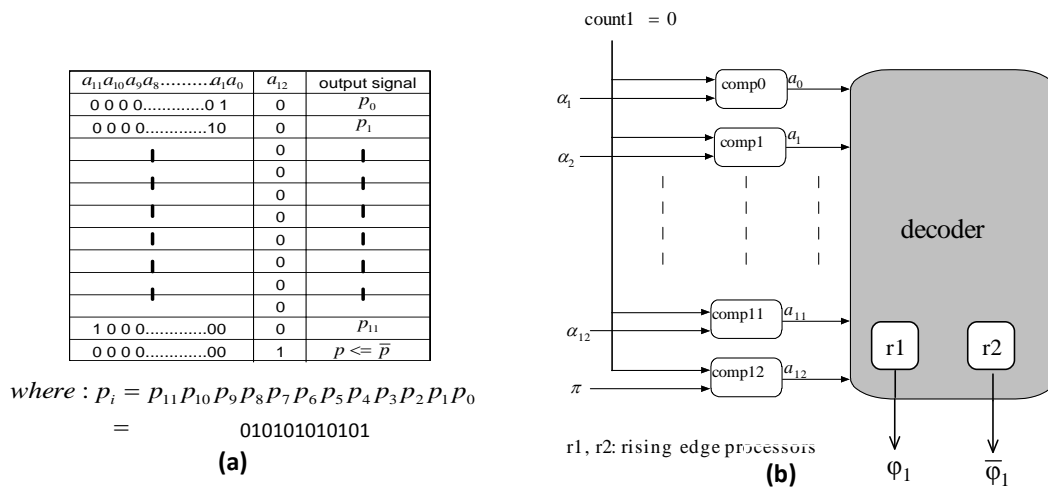
Figure(7) Decoding function generator for the first phase (a) pulse width modulated signal generator (b) decoding procedure

When the count value reaches α_2, the output signal is change to p_1, and so on. When the counter reaches to a value equivalent to π, the p_i register values are complemented and the counter is reset and starts counting again to synthesis the next half of the output signal. This operation continues as long as the chip power holds on, so that the output signal is periodically generated. The same procedure mention above is applied for the other two phases ($\Phi2$ and $\Phi3$).

From Fig.6 and Fig.7, one can see that for each phase, there are two output signals: the original PWM signal and its complements. The complemented signal is simply generated by using NOT gate. But the rising edge for both signals (the original and complemented) now becomes critical. Therefore, each rising edge state should be delayed for a specific duration of time for either original signal or complemented one. Thus, a special processing is achieved in the decoding part of the decoding function generator. A delay is added for each state before it setting to '1' (see Fig. 8 and Fig. 9).
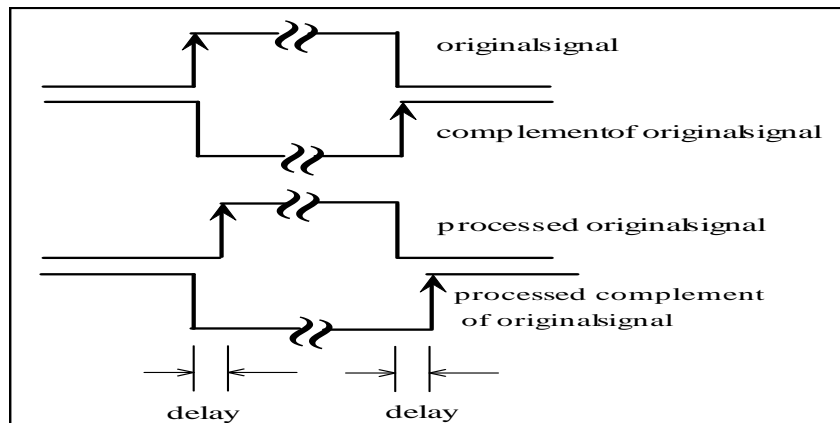
Figure(8) How to process the rising edge state
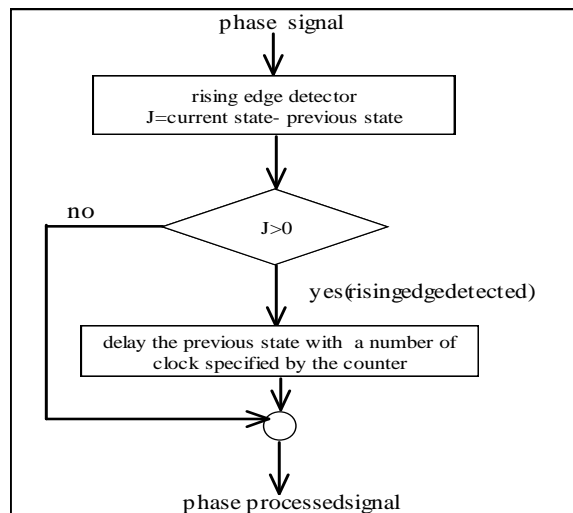
Figure(9) Flow chart of the rising edge

The experiential results have been chosen to describe some features of the hardware model of PWM generated using Xilinx Spartan-3E FPGA of 500,000 gates. Each of the design

architecture is modeled by using VHDL language and implement through ISE 9.2i program as a target technique. A comparison was made among three states for generation of switching angles for different modulation indexes. These states are for off line mathematical, neural network and neural network based FPGA modules. This comparison is clearly depicted in Fig. 10
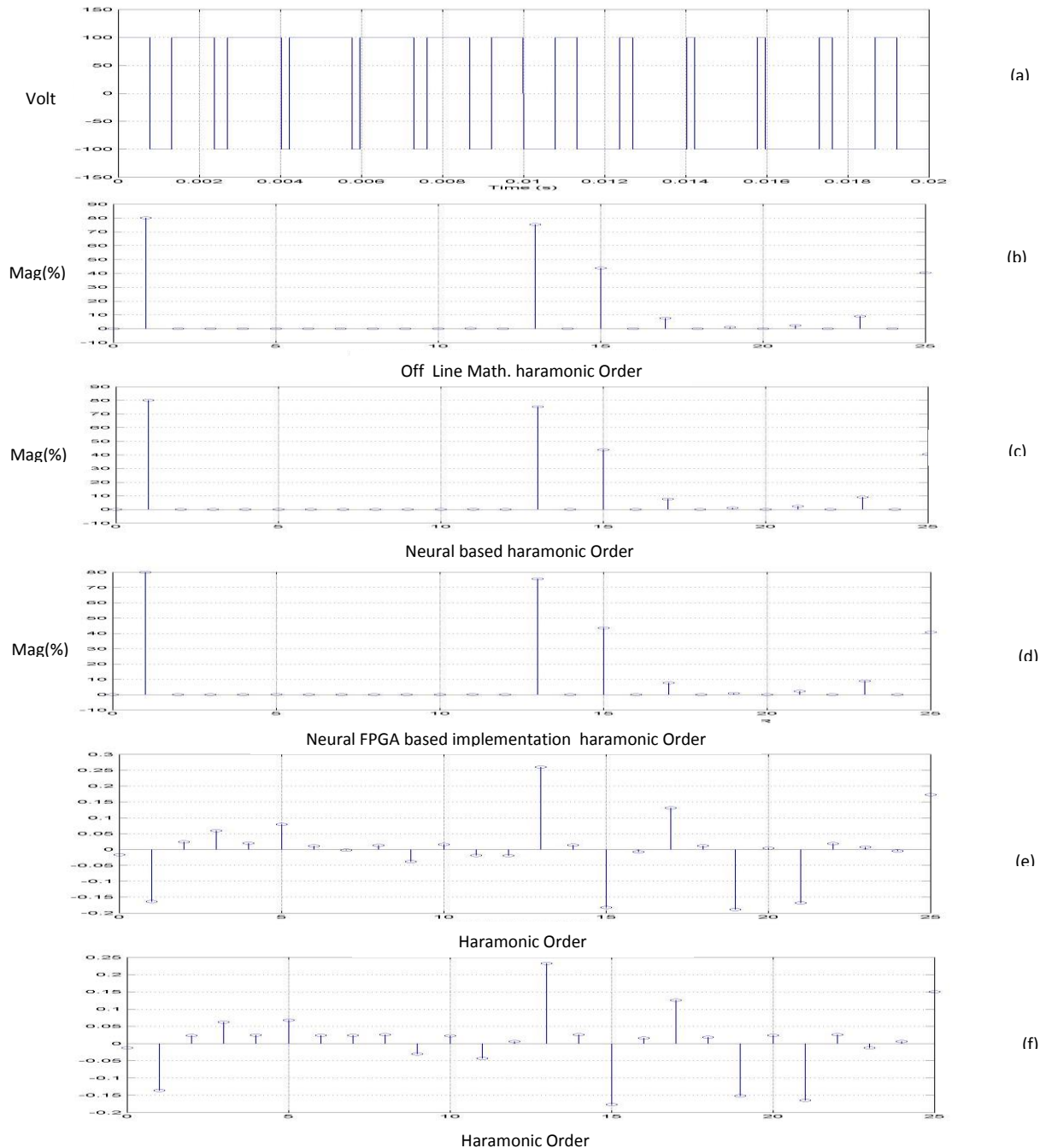

Figure (10). (a). The output voltage of the inverter with M=0.8,   (b). The FFT spectrum off-line mathematical state, (c). The FFT spectrum using software model of neural network, (d). The FFT spectrum using FPGA hardware model of neural network, (e). Spectrum difference between off line math and software neural state, (f) Spectrum difference between software neural state and FPGA hardware neural state.

7. Experimental Results

As mentioned the last paragraph, the device chosen is the Spartan 3E, which contains 4656 slices, 20 embedded multipliers, and has maximum clock rate of 50MHz. Area and speed are the two main measurements in evaluating system performance of the proposed system. The area is measured by number of FPGA slices and embedded components occupied. Speed is measured by the maximum allowable clock frequency. Table I presents the utilization summary of the Spartan-3E (XC3S500E) chip when the word length is set to 18 bits. The FPGA resources shown in this table are exploited from all units of the designed architecture shown in Fig. 6c.

TABLE I

UTILIZATION SUMMARY FOR SHEPWM NEURAL NETWORK BASED SYSTEM IN THE SELECTED DEVICE SPARTAN-3E (XC3S500E)

Component	NUMBER	%Utilization
Slices	1433 out of 4656	30%
Slice Flip Flops	576 out of 9312	6%
4 input LUTs	2440 out of 9312	26%
MULT18X18s	8 out of 20	40%

T_d : time delay

T_M : full period time

f_{iTd} : i^{th} harmonic component when the time delay is added

f_{10} : first harmonic component without time delay.

From this table, it can be notice that 8 out of 20 multipliers are only used. One multiplier is used in a pipeline manner to multiply M by the weights of the input layer. Another multiplier is used in the approximated Tansig Activation Function and six multipliers are used for each neuron in the output layer. 30% slices can be consider as a reasonable consumption of gates.

The system can operate on maximum frequency which equal to 55.737MHz. But the actual system frequency for the clock cycle is 50MHz which is limited to the Spatan 3E model used in this paper.

Fig. 11 shows the voltage of the inverter with the value of modulation index M=0.8 and the same Fast Fourier Transform (FFT) spectrums for three phase signals. Table II shows the THD for both voltage and inductive load current at different modulation index values.

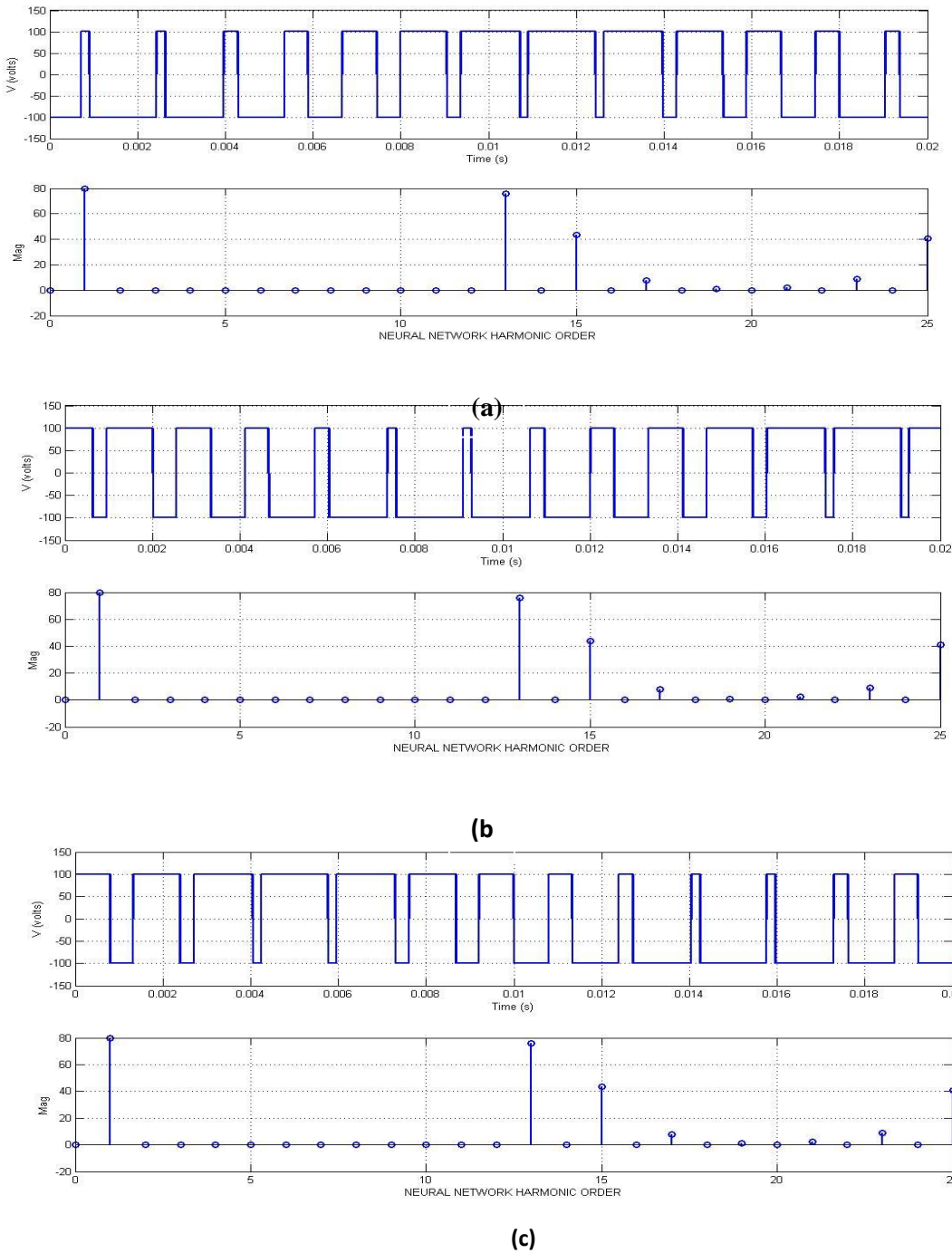**TABLE II: TOTAL HARMONIC DISTORTION FOR VOLTAGE AND CURRENT**

M	THDv	THDi
0.3	1.38 %	0.4 %
0.5	1.62 %	0.59 %
0.9	1.31 %	0.29 %

M   :Modulation index

THDv :Total Harmonic Distortion for Voltage

THDi :Total Harmonic Distortion for Current

at f=50Hz, L=5 mH, R=5Ω, # harmonics=13

(a)

(b

(c)

Figure(11) The output voltage of the inverter and its FFT spectrum for (a) phase1 at M=0.8 (b) phase2 at M=0.8 (c) phase3 at M=0.8.

In Table III, it can be seen that with the increasing of the rising edge time delay, the resolution still acceptable. The first harmonic component is considered as a reference in the comparison of table III.

TABLE III
**COMPARISON OF FREQUENCY COMPONENTS WITH AND WITHOUT ADDED TIME DELAY**

$\dfrac{T_d}{T_M}$ %	$\dfrac{f_{1\,Td}}{f_{10}}$	$\dfrac{f_{3\,Td}}{f_{10}}$	$\dfrac{f_{5\,Td}}{f_{10}}$	$\dfrac{f_{7\,Td}}{f_{10}}$	$\dfrac{f_{9\,Td}}{f_{10}}$	$\dfrac{f_{11\,Td}}{f_{10}}$	$\dfrac{f_{13\,Td}}{f_{10}}$	$\dfrac{f_{15\,Td}}{f_{10}}$
0%	1	0.0009	0.00096	0.00011	0.0007	0.0011	0.9466	0.5456
0.0016%	1.0001	0.0081	0.0081	0.0079	0.0080	0.0081	0.9446	0.5441
0.0032%	1.0002	0.0160	0.0160	0.0158	0.0159	0.0160	0.9387	0.5397
0.0048%	1.0003	0.0240	0.0239	0.0238	0.0238	0.0239	0.9289	0.5323

T_d : time delay
T_M : full period time
$f_{i\,Td}$: i^{th} harmonic component when the time delay is added
f_{10} : first harmonic component without time delay.

In Fig. 12a, one can be notice that every phase signal changes its state at the same time with its complement (q000:q180,q060:q240,q120:q300). After rising edge processing, the case that has seen in Fig.8 can be clearly recognized in Fig.12b (q_000:q_180,q_060:q_240,q_120: q_300). In Fig.12a, one can also see that the 2nd and 3rd phase signals start synthesis when the signals start1, and start2 become active. Then count1 and count2 start counting respectively according to the count value of the global counter.

8. Conclusion

A reliable real time system to generate pulse width modulation (PWM) signals with selected harmonic elimination(SHE) by using FPGA to derive three single phase VSI is presented. Neurons in all layers of the neural network for SHEPWM are processed in parallel. That is due to the pipelined and parallel architecture of the proposed system. The system generates the switching angles for all phase in very short time. All switching angles required for all phases can be concluded from the six fundamental angles produced by neural network hardware, which is used for single phase. Thus, a reduced chip area is used to implement the design. Either the spectrum differences of the proposed hardware system with the off line mathematical or software version of the neural based systems is minimized. This is due to the fixed point calculations that achieved in high resolution.

(a)

(b)
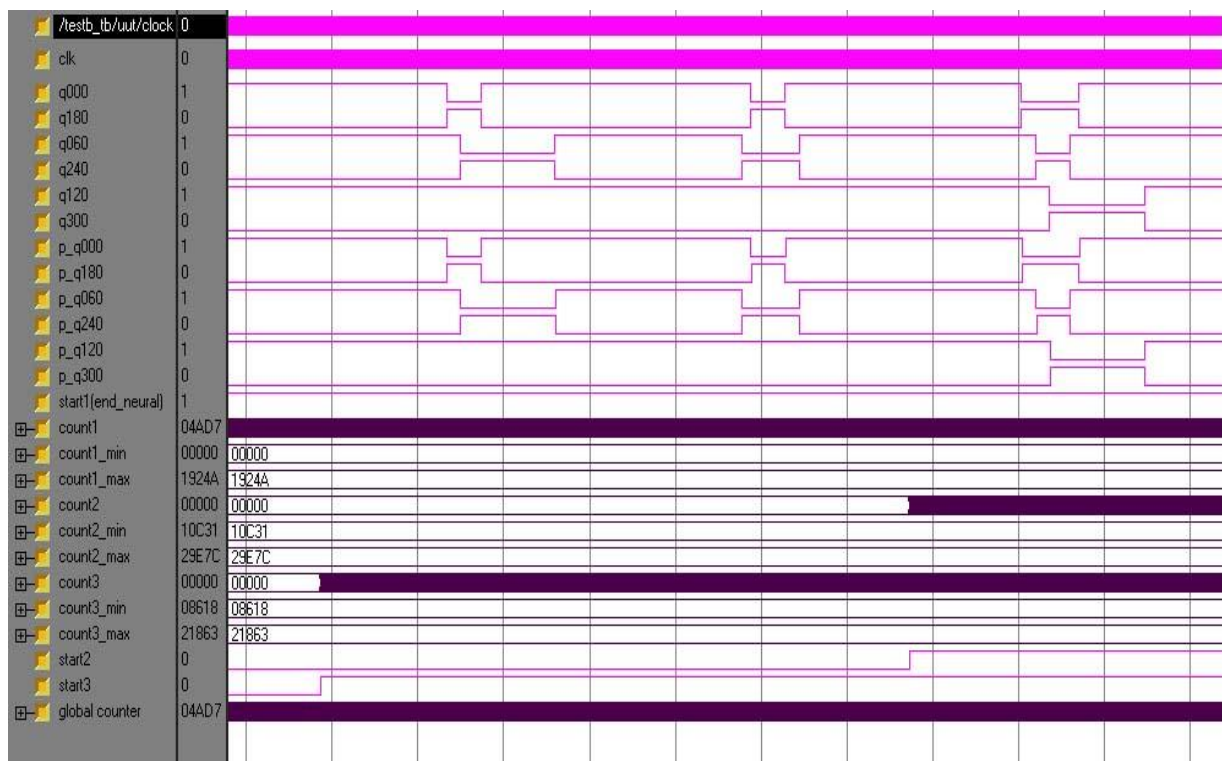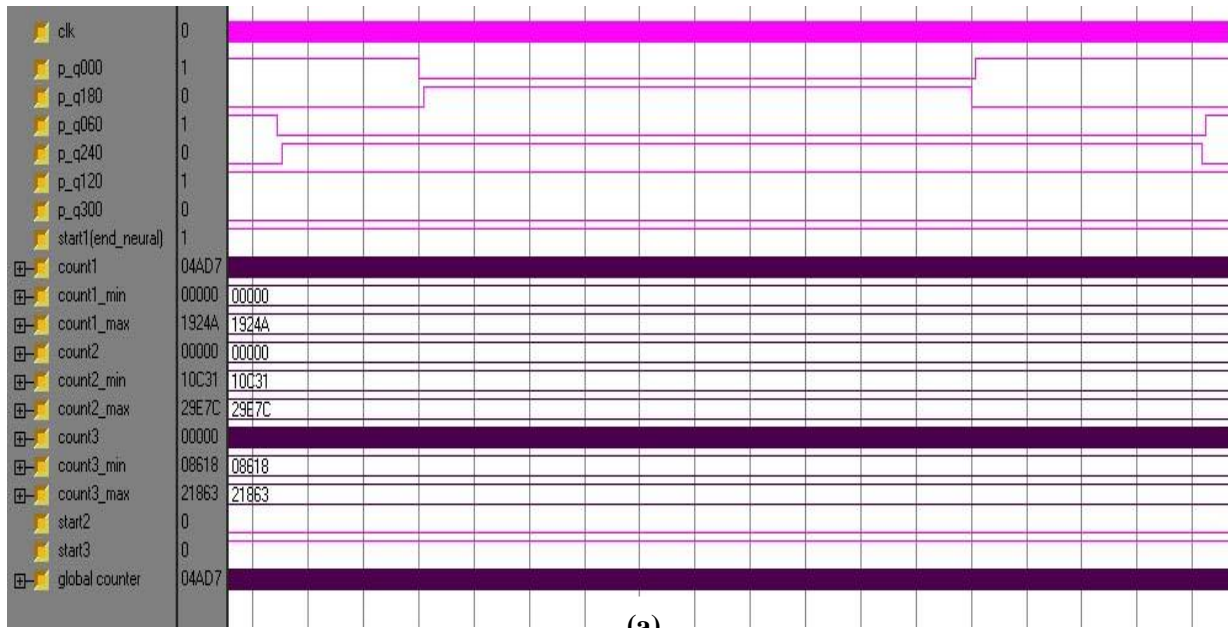
Highly compressed clock state

Highly compressed changed values

Figure(12) (a) The timing diagram of the SHEPWM system for three single phase signal. b) Enlarged timing diagram shows the delay of rising edge state.

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