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Efficiency Enhancement of CMOS Power Amplifier for RF Applications

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ABSTRACT

This paper presented a new structure for the CMOS power amplifiers as a more effective trend to amplify radio frequency (RF) signals compared to polar power amplifiers PA's by using envelope removal and restoration (EER) technique. Polar PA offers high-efficiency RF-modulated linear signal amplification. However, these amplifiers need high uniformity between the amplitude and phase of the modulated signals. The last translates promptly into higher energy consumption. Rather than deconstructing the quadrature signals into the combination of phase and amplitude signals, it is suggested that the CMOS quadrature power amplifier (QPA's) technique had been used to amplify RF signals immediately. The linearity, bandwidth, efficiency, and power consumption of the QPA's has been improved by separate amplitude and phase quadrature signals. The quadratic geometry architecture contains two bridges from modulated PA's that are able to treat negative or positive voltages, modulation, and RF-power bundling.

The design of the new structure is compared with respect to parameters such as fundamental frequency, power gain, PAE, output power, technology or fabrication process, and number of stage transistors. Simulation results for PA's design using CMOS process show an effective quadrature model by a power-added-efficiency (PAE) of 78.413% at a maximum output power of 21.619dBm. The third intermodulation IDM3 is -49.2dBc at output power driven at frequency 2.4 GHz and input power greater than 20dBm. The amplitude and phase distortion has been obtained of 1.4 and 0.26 °/dB respectively at 50MHz of bandwidth for modulated signals.

Keywords:

CMOS power amplifier; Quadrature modulator; Class D Power amplifier; and power added efficiency.

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1. INTRODUCTION

The transceiver unit of any mobile communication systems consists of the transmitter and receiver. Wireless communication means sending and receiving signals to and from the antenna [1]. The one most important stage with the antenna in the transmitter unit is the power amplifier which needs effective efficiency and linearity. High efficiency and linearity are essential for an inexpensive transmitter for wireless systems. There are a lot of researchers like Hertz [2], Faraday [3], Maxwell [4], and Tesla [5] who participated in electromagnetic and wave theory. Fig. 1 represents a typical RF transmitter with direct conversion architecture [7]. There are many applications of the RF-PA's circuits such as radio communication system [8], television broadcasting [9], radar [10], and RF-heating. The classes of the PA design are A, B, C, D, E, and F which operate at different ranges of frequencies starting from low values to microwave range [11]. It is a critical component of drive units for communication systems and is expected to provide adequate power output that arrives to megawatts depending on the application. The output power of the PAs must be sufficient for reliable transmission with high efficiency, gain, and good linearity. The number of amplifier stages decreases by increasing gain. It is required to transmit the output power generated from the transmitter unit. Battery life, and thermal conduction have been improved by obtaining high efficiency. The bandwidth of the modulated

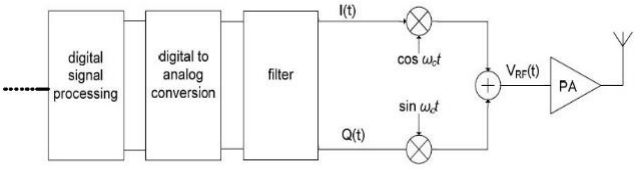

Fig. 1 RF transmitter with direct conversion architecture

signals produced from QPA's circuit through good linearity design [12].

The efficiency of the PA is an important factor for the overall performance of the wireless design. Therefore, switch-mode-PA's have been progressed to obtain high efficiency when the PA operates at a higher range of frequency but it is driven by constant signals. Whereas, due to the growing demand for high-speed data transmissions in wireless communications [13]. There are some new modulation schemes that have been introduced without generating a more constant envelope signal, but with a high to average peak power signal [14]. Therefore, a new technique, called quadrature modulation, has recently been proposed to efficiently operate power amplifiers in switch-mode while being driven by a high to medium peak power [15].

There are many researches published on this field. First of 2009, C.H. Lee et al. in [16] introduced a new architecture of PA's by using EER method in order to amplify RF modulated signals compared to conventional polar power amplifiers. They show a functional quadrupole model operated in 2.4 GHz with an additional 30% energy efficiency at maximum output power of 6.4dBm and bandwidth of 10MHz. While with 50MHz bandwidth of PAs, the PAE of 25% at 5.1dBm power. But the quadrature PA designed in this paper has a good PAE of about 78.413% with maximum output power of 21.613dBm and power input higher than 20dBm compared to [16].

Ildu Kim, and et al. in [17] proposed a new approach for a PAs design by using hybrid EER transmitter. ADS and MATLAB simulations have been used to realize this design utilizing a silicon LDMOSFET model. The total maximum PAE is 35.5% at an output power of 29.2dBm. The results have been obtained to show that the proposed structure of PA's is a good filter for effective linear transmitters.

Minoh Son and et al. in 2019 [18], proposed a balun embedded driver stage to improve the bandwidth of a differential CMOS PA. The design operates at 5 GHz for WLAN applications fabricated by 180-nm CMOS technology. Measured results at 4.7 GHz frequency show that the PAE is 10.16% at maximum output power of 20.18dBm. The bandwidth obtained is 20MHz.

In this study, ADS software has been used to design a new proposed structure of the RF power amplifiers that operated on high efficiency, good linearity, and quadrature type based on a CMOS process. The QPA contains two modulated signals that operate at 2.4GHz. The results obtained are very good and can be used at other frequencies such as 2.14GHz for mobile communications and 2.45GHz for wireless application. The design of the new structure is compared with respect to parameters such as fundamental frequency, power gain, PAE, output power, technology or fabrication process, and number of stage transistors. The parameters obtained are then compared with other literature reviews using a table and the different parameters of the different designs are plotted graphically for comparison.

2. CMOS POWER AMPLIFIER

In switched-mode PAs, the switch represents an active device and has no dispersed power because of the voltage drop and current flow by switch are zero. So, the transistor's efficiency is 100% via it's no power consumption. Class D and E are non-linear amplifiers [22]. Class-D PA involves a load network and two transistor switches that lie between ground and voltage source. The Class-D is appropriate for voltage modulation through the direct connection between the output of the amplifier and the source of the supply. Envelope elimination and restoration EER technique has been used to improve linearity of the amplifiers. The EER is the motive for the QPA architecture [23].

QPA is a new structure of PA's and it has been presented as a more energy effective method of amplifying radio frequency modulated signals compared to traditional methods. Quadrature signals such as the message signals I(t) and Q(t) can be directly amplified and modulated with the RF carrier signal using QPA without deconstructing the signal into groups of phase and amplitude. The lack of a phase separation and amplitude signal path avoids linearity and bandwidth requirements.

2.1. Quadrature Signals

The modulated RF signal is described as:

$$V_{RF}(t) = A(t)\sin(\omega t + \emptyset(t)) \quad \ldots\ldots (1)$$

But written as

$$V_{RF}(t) = I(t)\sin(\omega t) - Q(t)cos(\omega t) \quad \ldots\ldots (2)$$

Where $I(t)$ and $Q(t)$ are quadrature components. Also $A(t)\ and\ \emptyset(t)$ are the amplitude modulation and phase of the signal respectively. These signals are separated by using EER technique. Then QPA's integrate and modulate these signals to provide high efficiency as shown in Fig. 2 [24].

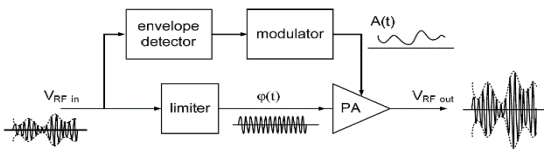

Fig. 2 Envelope Elimination and Restoration EER

However, the overall performance of the QPAs will be defective such as reduced linearity and bandwidth because of differential delays in signal paths after separation. To solve this limit, the QPA is used to modulate I(t) and Q(t) signals that the phase shift between them of 90° [25].

2.2. Quadrature PA's Configuration

The RF carrier signal I(t) and Q(t) is modulated at 2.4 GHz by using power amplifiers such as class D or class E are described in Eqs. (3) and (4). These configurations are appropriate for modulating the voltage supply between V_{DD} and V_{SS} to produce the RF desired signals. Class D was chosen in this work because of its high efficiency, and it is provided by a constant voltage (V_{DD} = 1.2V) and duty cycle of 50%. The operation of the PA is push-pull and it doesn't open or close at the same time. Fig. 3 shows two symmetrical PA switches. The resistive load R_L is connected between them and causes the two output voltages to differ in load. The filter is tuned to the RF frequency according to value of the LCR network L=33nH and C=0.133pF as reported in Eq. (5).

$$I(t) = A(t)\cos(\emptyset(t)) \quad \text{……. (3)}$$

$$Q(t) = A(t)\sin(\emptyset(t)) \quad \text{……. (4)}$$

$$\omega = \frac{1}{\sqrt{LC}} \quad \text{……. (5)}$$

A sinusoidal output is produced by a first order LC filter with a low reactance to the fundamental and a high impedance to the harmonics. The Fourier series of the input, assuming a pulse signal with a 50% duty cycle is explained in Eq. (6).

$$V_{out} = \frac{2V_{DD}}{\pi}\sum_{k=1}^{\infty}\frac{\sin((2k-1)2\pi ft)}{2k-1} \quad \text{… … … (6)}$$

To implement an ideal circuit in real time applications, transistors must be used to act as switches in order to minimize chip area and power consumption. To reduce body effect and loss, the volume can be changed to suit the appropriate volume voltage for the positive and/or negative I(t) signal. Fig. 4 shows the QPA's in bridge-mode, the bulk switches appended for the most part. Where the M_1, M_2, M_5, and M_6 are PMOS. The NMOS transistors are M_3, M_4, M_7, and M_8. Also Mb_1 to Mb_{16} are CMOS with bulk.

Active load draw technology is the rule of applying current from a source that has two phase correlations which can change the RF load to represent resistance or reaction. Load pull is a technique in which the device under test DUT observes the resistance of the load. DUTs are varied and their performance is measured simultaneously [26]. Similarly, source pull is measured for various source impedance. The results are helpful in calculating the optimal source and load impedance to provide the best performance [27].

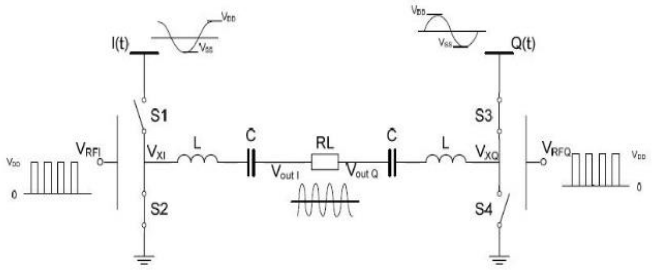

Fig. 3 QPA design using ideal switches.

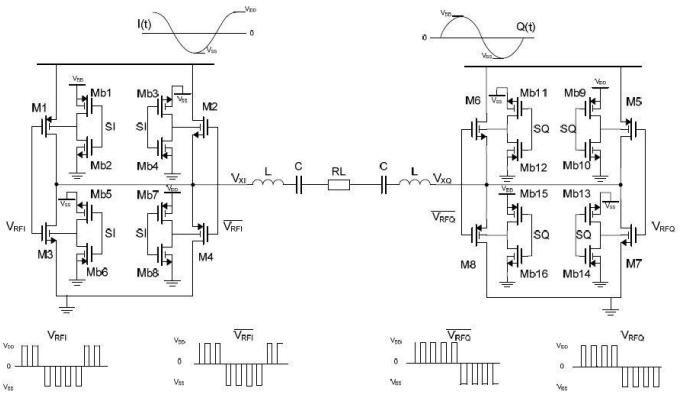

Fig. 4 QPA design using bulk switches.

In this design, active load pull and source pull devices have been completed for effective and optimum efficiency. The simulation results clear that the optimal value of the load resistance and reactance is 14.771 + j* 13.34 Ω. For maximum power transmission because a correspondence is made between the impedance of QPA output and 50 Ω load. The optimal value of input impedance for QPA is 25.35 + j*21.878 Ω for maximum power transmission. The load and source impedances have been used for design of matching network for input and output circuits of the QPA. These networks are discussed in simulation sections.

3. DESIGN AND SIMULATION OF CMOS QPA AND DISCUSSION RESULTS

The QPA model and driver are designed with 90nm CMOS technology that operates with a nominal source voltage V_{DD} = 1.2V and V_{SS} = -1.2V. In addition to the 90nm feature length devices, larger feature length L = 240 nm were used, but the channel width W depends on the manufacturing area process. QPA used in wireless WLAN (IEEE 802.11) which requires the RF

carrier frequency f_{RF} = 2.4 GHz and mobile communication systems. The simulation of a design was performed by using ADS update 2009.

There are many steps of the QPA amplifier design in ADS simulation such as choice bias supply voltages through DC simulation part, find the optimum impedances for input and output via design of matching networks, design of the driver circuit to drive QPA, and complete overall design of the QPA and find numerical results.

As above-mentioned, WLAN needs high linearity to provide more bandwidth and to high efficiency to realize modulation. The specifications of the QPA amplifier have been designed in this work for wireless LAN application as listed in Table 1 [28].

Table 1: Design specifications of PA's for WLAN

Operational center frequency [GHz]	2.4
Bandwidth per channel [MHz]	5-50
Maximum output power [dBm]	20-26
PAE% at maximum output power [%]	> 50%
IMD3 at maximum output power [dBc].	-20
IMD3 at 6dB back-off from maximum output power [dBc].	-30

3.1. Design of a QPA driver circuits

Quadrature-PA is controlled by a fixed RF pulse for both negative and positive edges, relying on the I(t) and Q(t) signals. The driver circuit contains a series of a set of switches with inverted output. The quadrature signals $S_{I(t)}$ and $S_{Q(t)}$ control the two groups of switches, one of them between V_{DD} and GND and the other between V_{SS} and ground. When I(t) are signed positive and negative, the signal is equal to V_{SS} and V_{DD} respectively. The output of the driver circuit is supply rails for the series of inverters. The driver architecture for a QPA is shown in Fig. 5.

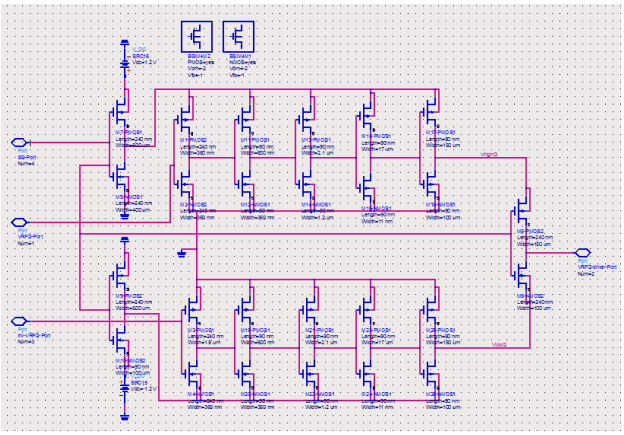

Fig. 5 Quadrature PAs driver circuit design

The architecture as shown in Fig. 5 is used to prevent the duplication issue when using both switches edges at the same time. It is controlled through the rising, and falling edges of the RF pulse supplied. The output of the QPA driver circuit compared to the input signal V_{RF} is shown in Fig. 6 for varied step sizes. Fig. 6 shows that at a certain step size, the output driver gives a 50% of duty cycle for RF pulse for both edges of switches. While in the other steps we couldn't find the output response. This leads to present losses such as switching and conduction loss. In order to decrease these losses and improve the efficiency, there must be reduced stages of the QPA driver circuits. It can be seen from Fig. 6, that the phase shift between two modulated signals is 90° and the output ripple occurred due to the size of the transistors and the effects of the unbalanced driver output resulting in a time of uneven rise and fall of the exit.

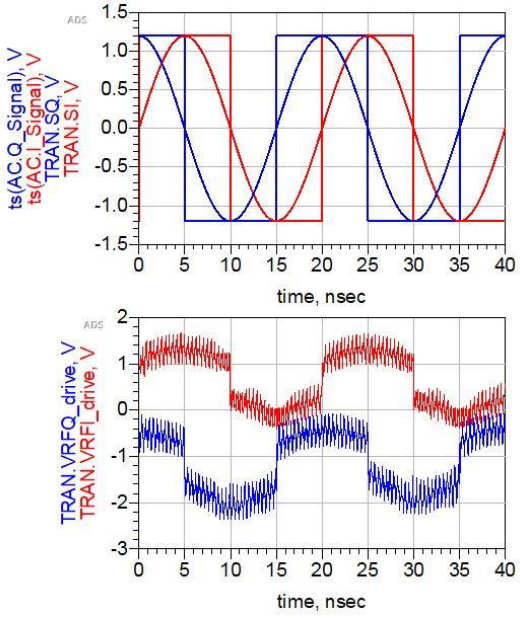

Fig. 6 output response of the driver QPA circuit for both signals I(t) and Q(t).

3.2. Matching Network Circuit

The input-output match can be provided using a simple match grid for discrete elements such as L-match, T-match, or π-match [25]. In this work the L correspondence was used to match the output between the output impedance (14.771 + j*13.4) Ω and the 50Ω load. The input correspondence between the input impedance (25.3 + j*21.878) Ω and 50 Ω source was used as shown in Figs 7 and 8 respectively. The quality factor Q of the finely tuned output network was chosen to select the corresponding circuit elements around 10, since higher harmonics produced from QPA design is low restraint and large value of

inductors due to low and high value of Q respectively. Very high Q results lower energy efficiency, smaller load is 50 Ω. The output signal is sinusoidal with no amplitude and phase distortions. Figures 9 and 10 represent the input and output match results for QPA using the L match network through the input and output reflection coefficients S_{11} and S_{22}, respectively. It is clear that the return loss at the input and output matching circuits are -7.77dB and -28.9dB respectively when the amplifier operates at a frequency of 2.4 GHz.

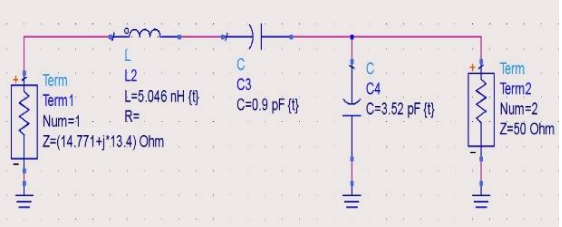

Fig. 7 Output matching network of the QPA

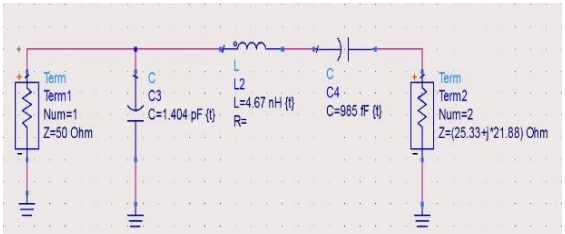

Fig. 8 Input matching network of the QPA

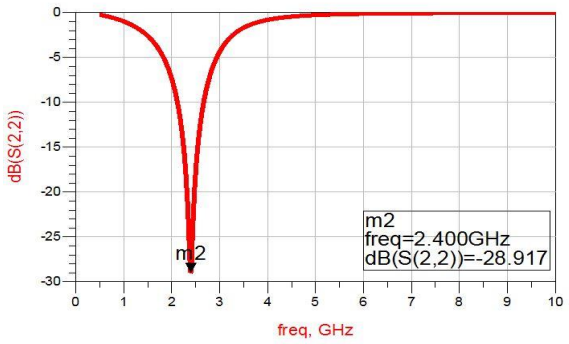

Fig. 9 Output reflection coefficient for input matching circuit of the QPA

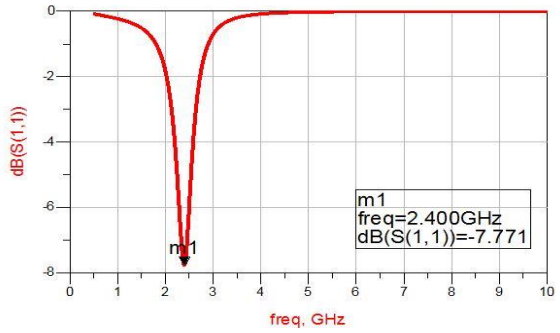

Fig. 10 Input reflection coefficient for output matching circuit of the QPA

3.3. Transient Analysis of QPA

The following simulations will be run for quadrature PA with and without bulk switches to test functionality and performance. A transient simulation was performed to verify the functionality of QPA. The I(t) and Q(t) signals were established as sine with a phase difference of 90°. These signals are carried out at the massage frequency f_{IQ} = 50MHz. The $S_{I(t)}$ and $S_{Q(t)}$ signals generated from the I(t) and Q(t) signals respectively are explained in Fig. 5.

The complete design of QPA's circuit consisting of two PAs with a quadrature modulation, a phase difference of 90° in bridge mode is shown in Fig. 11. The QPA output signal must not be stationary and filtered by the LCR, resulting in a sinusoidal shape in the same way. The maximum output voltage V_{out} = 510 mV. The envelope output voltage of the QPA is shown in Fig. 12.

3.4. Harmonic and distortion of the QPA

Harmonic balancing is a technique for analysis of the distortion for non-linear amplifier circuits by using frequency domain. It calculates the spectrum value of the voltage and current existence in a circuit and calculates the intersection point and intermodulation distortion. The QPA design overall circuit has been performed by using one-tone harmonic balance simulations. The simulation is used to calculate the numerical results such as maximum PAE% in the presence of interference sources.

The complete design of QPA was achieved to simulate a single tone using an ADS simulator. The amplifier has a very good PAE of 78.4% at maximum output power 21.6dBm as shown in Fig. 13 m_6 point. Also, the QPA's has high-linearity and low cross-sectional distortion, see spectrum signal at the frequency of 2.4 GHz in Fig. 14. It is clear from the figure that the output spectrum is 13dBm at the fundamental frequency through the m_4 point, while at the second harmonic of the spectrum m_5 point the output is -33.5dBm. Figure 15 explained the amplitude and phase distortion has been obtained in this design as a minimum value about 1.4 dB/dB and 0.26 °/dB respectively at output power 21.619dBm.

Based on the results that obtained in this work, we can have presented a table. Table 2 describes a comparison of this work with some literature review in this field. It's clear from the table that the QPA structure of the PA's gives the best performance for amplifiers in RF applications at a resonance frequency of 2.4GHz.

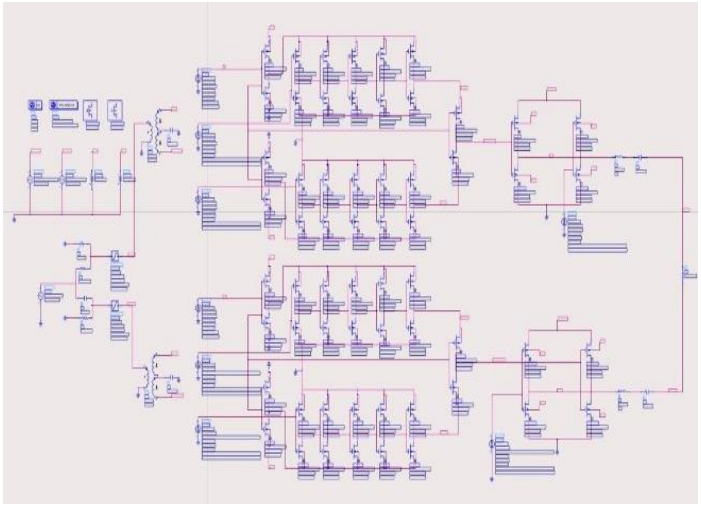

Fig. 11 Schematic design of full Quadrature power amplifier circuit with driver modulated signal

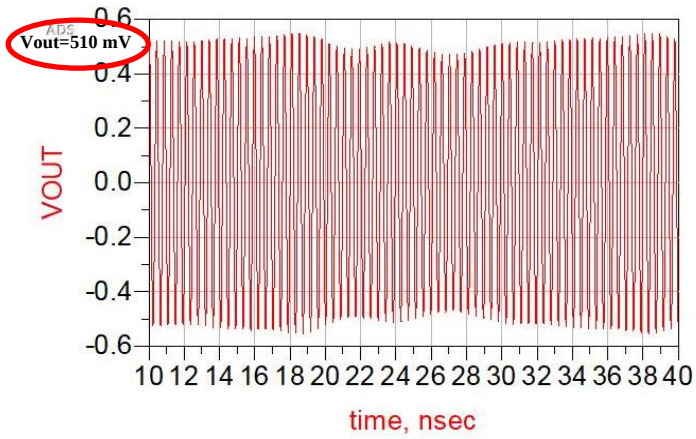

Fig. 12 Simulation results for QPA output with sinusoid I(t) and Q(t) at 50 MHz bandwidth

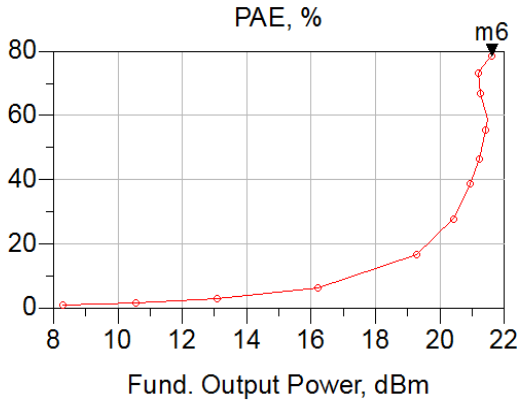

Fig. 13 QPA's PAE of 78.4% designed at maximum power output of 21.619 dBm

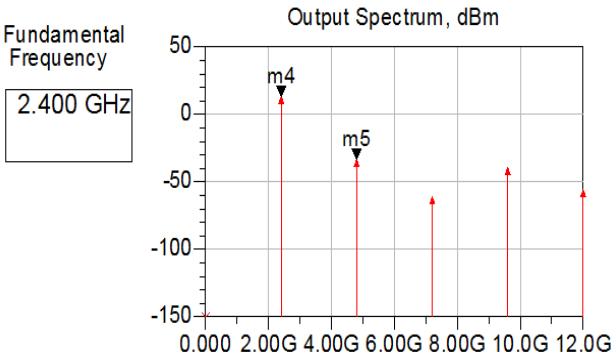

Fig. 14 QPA output spectrum design when IDM3 is -49.2dBc at maximum output power

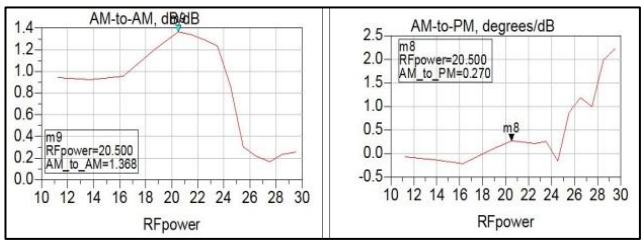

Fig. 15 Amplitude and phase distortion of the QPA designed at input power is more than 20dBm

Table 2: Summary comparison this study with literature reviews

Parameters	[19]	[20]	[21]	This work
Process	MOS	MOS	MOS	CMOS
Technique	EER	ER	H-EER	EER
Freq., [GHz]	2.4	2.3	2.4	2.4
PAE, [%]	28	44.4	60	78.413
Gain, [dB]	6.5	8.4	6.5	7.1
Output power [dBm]	19	20.41	19	21.619
Bandwidth [MHz]	20	Broad band	20	50
Bias voltage	0-4	0.6-0.72	0-5.5	±1.2

4. CONCLUSION

A quadrature power amplifier QPA concept was introduced as a modification to traditional power amplifiers by using envelope elimination and restoration EER technique. This idea was developed into an effective model at the transistor levels. The numerical simulation shows that QPA is capable of handling quadratic signal operations in the RF band.

CMOS technology has been used in this work to design both QPA and driver circuit at operated biasing supply voltages V_{DD}=1.2 V, V_{SS}=-1.2 V, operating RF frequency f_{RF}=2.4GHz. 240nm CMOS process used for larger devices.

The time and frequency domain analysis of the QPA were calculated at variant frequency

bands. As the showed that the QPA amplifier could be operated at WCDMA base station and wireless WLAN when the level of input power is more than 20dBm. The amplifier has good efficiency with a PAE of 78.413% at f_{IQ}=50MHz bandwidth message of the quadrature signals. Also it has a good output spectrum at 2.4 GHz about 33.5dBm is shown on Fig. 14 and third harmonic intermodulation spectrum IDM3 is less than the main spectrum by 20dBm. The IDM3 obtained is -49.2dBc at maximum output power of 21.619dBm. The amplitude distortion is about 1.4 dB/dB, and phase distortion about 0.26deg/dB.

Appendix: Nomenclatures, Greek Symbols, and Abbreviations were used in this study

EER	Envelope Elimination and Restoration.
H-EER	Hybrid-EER.
IMD3	Third harmonic intermodulation spectrum.
I(t), Q(t)	RF Modulated sugnals I and Q sides.
PAE	Power-Added-Efficiency.
QPA's	Quadrature Power Amplifier.
RF	Radio Frequency.
S_{11}, S_{22}	Output and input reflection coefficients.
V_{DD}, V_{SS}	Supply voltages of the QPA design.
Vout(I), Vout (Q)	Output voltage for both phase (I and Q) of QPA.

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تحسين كفاءة مكبر قدرة نوع CMOS لتطبيقات الترددات الراديوية

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الملخص

تم اقتراح بنية جديدة لتصميم مكبر او مضخم قدرة نوع QPA بتقنية CMOS كطريقة أكثر فاعلية لتضخيم الإشارات المعدلة بترددات الراديوية مقارنة بمكبرات قدرة القطبية التقليدية (Polar PA's). تم ذلك باستخدام تقنية إزالة المغلفات واستعادتها (EER) وبكفاءة عالية، توفر الـ Polar PA تضخيمًا خطيًا للإشارة معدلة ذات التردد الراديوي عالي الكفاءة. ومع ذلك، تتطلب هذه الأنظمة محاذاة عالية بين مساري إشارة الاتساع والطور، ويجب أن يكون عرض النطاق الترددي لمسار الاتساع أكبر بثلاث إلى أربع مرات من عرض نطاق الراديوي. وبالأخير يؤدي مباشرةً إلى ازدياد استهلاك الطاقة. بدلاً من تفكيك إشارات المضمنة إلى مزيج من إشارات الطور والسعة، يُقترح أن يتم تضخيم الإشارات المضمنة مباشرةً باستخدام QPA. وان عدم وجود مسار إشارة الطور والسعة المنفصلين يؤدي إلى تجنب متطلبات الخطية وعرض النطاق، مما يقلل من استهلاك الطاقة. يتم تقديم تقنية التضمين محتملة لـ PA والتي تتكون من مضخمين للطاقة في وضع التبديل الجسري بحيث يمكنهما التعامل مع الفولتيات السالبة والموجبة وتجميع طاقة الترددات الراديوية. بالإضافة إلى ذلك، يتم التحكم بشكل صحيح مع QPA.

تتم مقارنة تصميم الهيكل الجديد فيما يتعلق بالمعاملات مثل لتردد العمل الأساسي، وكسب الطاقة، وPAE، وطاقة الإخراج، والتكنولوجيا المستخدمة أو عملية التصنيع، وعدد الترانزستورات المرحلة. تُظهر نتائج المحاكاة الخاصة بـ PA باستخدام تقنية CMOS بان كفاءة مضافة للطاقة بنسبة 78.413% ومعدل التضمين التداخلي IDM3 هو (62.6 dBm-) عند (21.619 dBm) كحد أقصى من طاقة الإخراج مدفوعة عند 2.4 GHz وطاقة إدخال أكبر من 20 dBm. تم الحصول على تشوه في السعة في هذا العمل حوالي (1.4 dB/dB)، وتشويه في الطور حوالي (0.26 Deg/dB) عند عرض النطاق الترددي للإشارة المضمنة الراديوية يساوي 50MHz.

الكلمات الداله:

مكبرات القدرة نوع CMOS، معدلات او التضمين نوع الرباعي، مكبر قدرة التقليدي نوع D، كفاءة القدرة المضافة PAE.